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1 This file contains the logic necessary for a GAL16V8 to decode latched
2 data bits D0-D2 and generate the CAS signals for the eight 256K banks of
3 memory (SIMMs) on the Micro Innovations 1MB/2MB memory board.
4
5
6 GAL16V8 1: DL2, 2: DL3, 3: DL4, 4: CASIN,
7          12: CAS1, 13: CAS2, 14: CAS3, 15: CAS4,
8          16: CAS5, 17: CAS6, 18: CAS7, 19: CAS8
9
10         Low: CASIN, CAS[1..8]
11
12         CAS1 = CASIN & DL[4..2]==0
13         CAS2 = CASIN & DL[4..2]==1
14         CAS3 = CASIN & DL[4..2]==2
15         CAS4 = CASIN & DL[4..2]==3
16         CAS5 = CASIN & DL[4..2]==4
17         CAS6 = CASIN & DL[4..2]==5
18         CAS7 = CASIN & DL[4..2]==6
19         CAS8 = CASIN & DL[4..2]==7
20
21
22         Signature: "2MU2rev0"
I289 Complex GAL architecture selected.

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RESOLVED EXPRESSIONS (Reduction 2)

Signal name	Row	Terms
CAS1	57	DL2' DL3' DL4' CASIN
CAS2	49	DL2 DL3' DL4' CASIN
CAS3	41	DL2' DL3 DL4' CASIN
CAS4	33	DL2 DL3 DL4' CASIN
CAS5	25	DL2' DL3' DL4 CASIN
CAS6	17	DL2 DL3' DL4 CASIN
CAS7	9	DL2' DL3 DL4 CASIN
CAS8	1	DL2 DL3 DL4 CASIN

♀ SIGNAL ASSIGNMENT

Pin	Signal name	Column	Rows			Activity	
			-----	Beg	Avail	Used	
1.	DL2	2	-	-	-	High	(Clock)
2.	DL3	0	-	-	-	High	
3.	DL4	4	-	-	-	High	
4.	CASIN	9	-	-	-	Low	
5.	-	12	-	-	-		
6.	-	16	-	-	-		
7.	-	20	-	-	-		

2MU2V8. LST						
8.	-	24	-	-	-	
9.	-	28	-	-	-	
11.	-	30	-	-	-	(Enable)
12.	CAS1	1	56	8	1	Low (Three-state)
13.	CAS2	27	48	8	1	Low (Three-state)
14.	CAS3	23	40	8	1	Low (Three-state)
15.	CAS4	19	32	8	1	Low (Three-state)
16.	CAS5	15	24	8	1	Low (Three-state)
17.	CAS6	11	16	8	1	Low (Three-state)
18.	CAS7	7	8	8	1	Low (Three-state)
19.	CAS8	1	0	8	1	Low (Three-state)
			-----	-----		
			64	8	(13%)	

I 200 No fatal errors found in source code.
I 201 No warnings.

♀OrCAD PLD-386
Type: GAL16V8
*

QP20* QF2194* QV1024*
FO*
L0000 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 *
L0032 01 01 01 11 10 11 11 11 11 11 11 11 11 11 11 11 *
L0256 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 *
L0288 01 10 01 11 10 11 11 11 11 11 11 11 11 11 11 11 *
L0512 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 *
L0544 10 01 01 11 10 11 11 11 11 11 11 11 11 11 11 11 *
L0768 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 *
L0800 10 10 01 11 10 11 11 11 11 11 11 11 11 11 11 11 *
L1024 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 *
L1056 01 01 10 11 10 11 11 11 11 11 11 11 11 11 11 11 *
L1280 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 *
L1312 01 10 10 11 10 11 11 11 11 11 11 11 11 11 11 11 *
L1536 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 *
L1568 10 01 10 11 10 11 11 11 11 11 11 11 11 11 11 11 *
L1792 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 *
L1824 10 10 10 11 10 11 11 11 11 11 11 11 11 11 11 11 *
L2048 00 00 00 00 00 11 00 10 01 00 11 01 01 01 01 01 *
L2080 00 11 00 10 01 11 00 10 01 10 01 01 01 11 01 10 *
L2112 00 11 00 00 11 11 11 11 11 11 11 11 11 11 11 11 *
L2144 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 *
L2176 11 11 11 11 11 11 11 11 11 11 *
C4B10*

I 202 5/4/92 5:49 pm (Monday)
I 203 Memory usage 17K
I 204 Elapsed time 1 second

♀
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