CHAPTER 2: HARDWARE

1. Introduction

This chapter presents technical information on each of the major logical components of ADAM identified in the System Block Diagram, Figure 2-1. The Appendix contains schematics and component location/identification drawings.

For the convenience of hardware developers, pin and signal connections for all expansion connectors are given. The Memory Console provides a total of four expansion connectors. Three female card edge connectors are accessed by removing the top cover of the Memory Console. These are referred to as expansion connectors #1, #2 and #3. One male card edge connector extends from the right side of the Memory Console. This is referred to as the Expansion Port.

FIGURE 2-1: SYSTEM BLOCK DIAGRAM

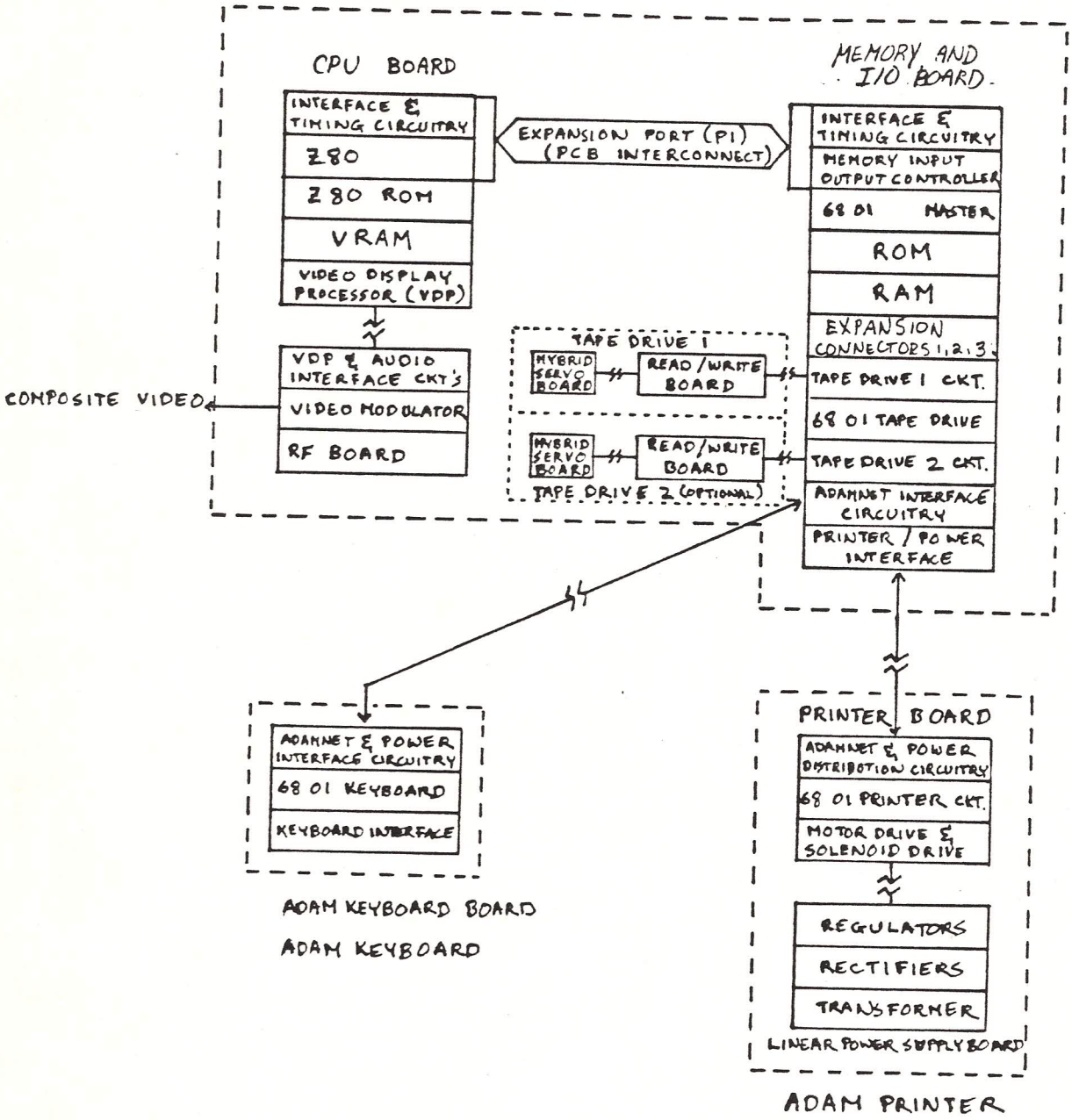
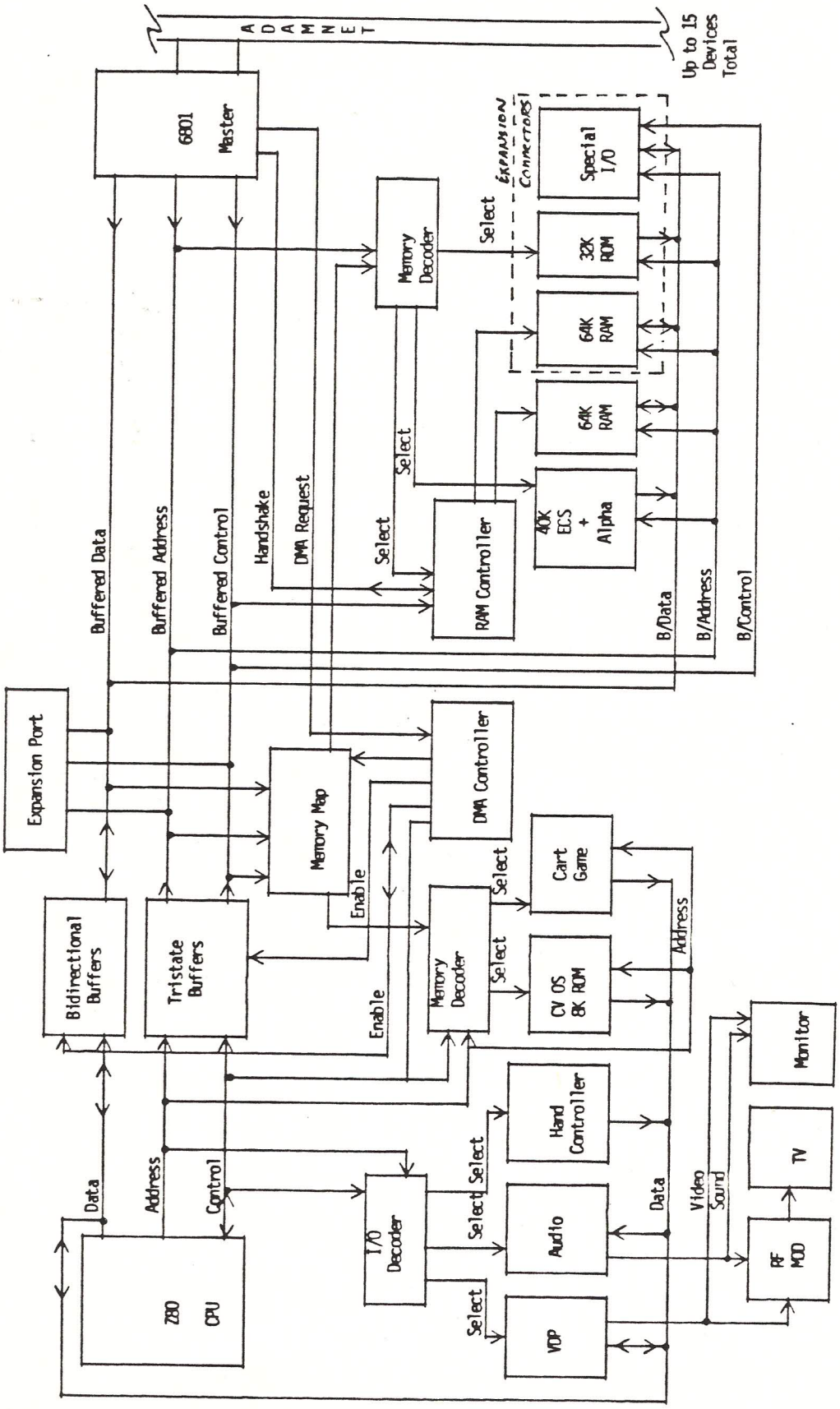


FIGURE 2-2: SYSTEM FLOW DIAGRAM



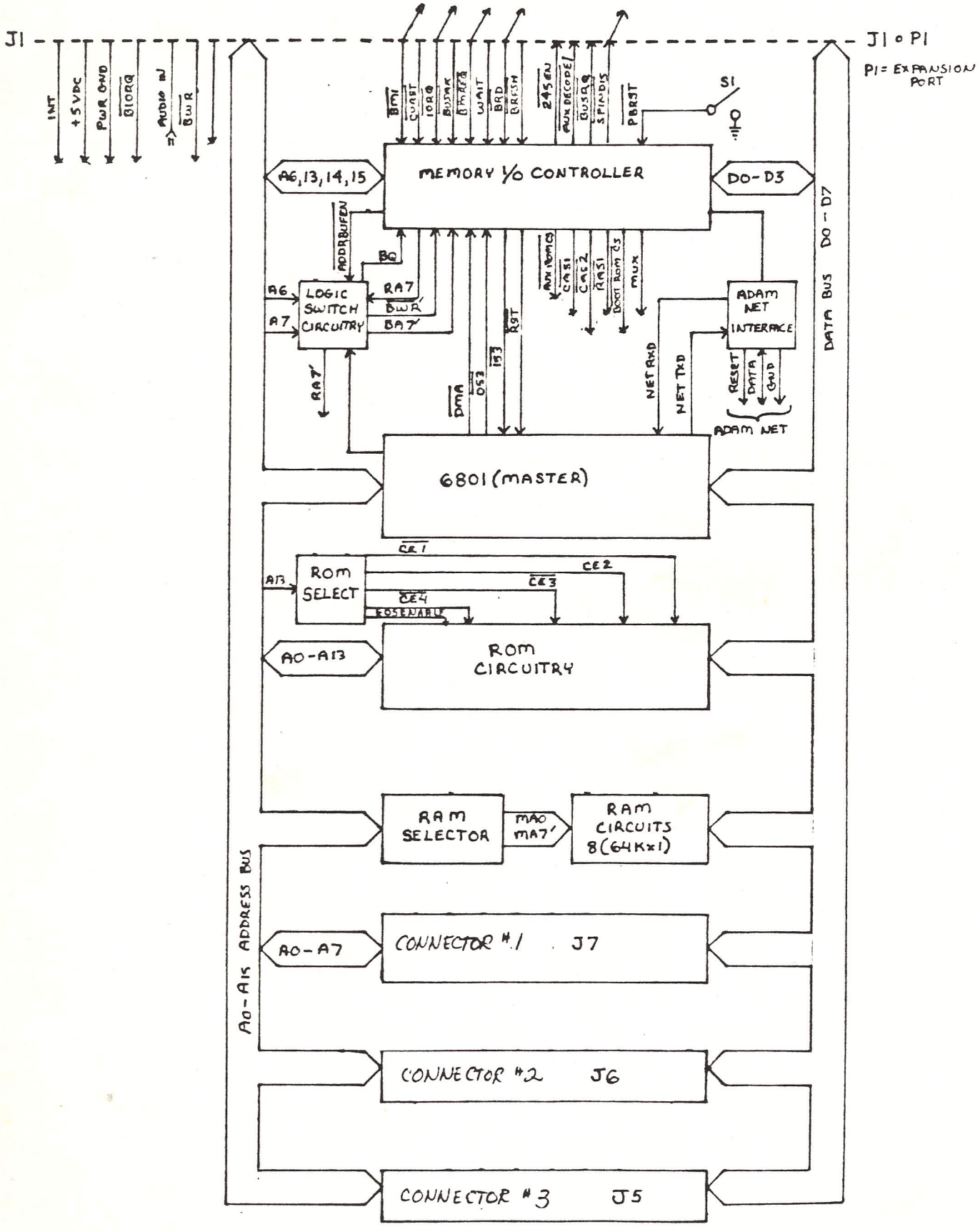
2. THE MEMORY CONSOLE

2.1 The Memory and I/O Printed Circuit Board

2.1.1 Theory of Operation

The Memory and I/O Board contains the 6801 Master microcomputer, 72K bytes of RAM and provisions for up to 72K of ROM/EPROM. This board provides the circuitry required to interface the keyboard, printer, tape drive and future options. Three card-edge connectors provide access for future options. An expansion port provides access for external peripherals. A custom LSI circuit, the Memory Input Output Controller (MIOC), interfaces the 6801 Master microcomputer with the Z80 microprocessor on the CPU Board. Another 6801 microcomputer on the Memory and I/O Board controls the operation of the tape drive interface cir cuitry.

FIGURE 2-2: THE MEMORY AND I/O BOARD BLOCK DIAGRAM



2.1.2 The Master 6801 Microcomputer

The Master 6801 microcomputer's primary function is to control system access to the keyboard, printer, tape drive and future peripherals. The Master 6801 microcomputer is a front end network processor that supports the Z80. The Master 6801 communicates with the Z80 via the Memory Input Output Controller. The Master 6801 reads and writes information to and from network peripherals on command by the Z80.

The 6801 chip provides 2048 bytes of ROM, 128 bytes of RAM and a UART. The Master 6801 is configured for single chip mode operation and runs, as do Adam's other 6801's, at a 1MHZ rate. This frequency is derived from an external 4MHZ crystal and the 6801's internal divide-by-4 circuitry.

2.1.3 The Memory Input Output Controller (MIOC)

The Memory Input Output Controller is a 40-pin IC that interfaces two dissimilar microprocessers (the Z80 and the Master 6801) by performing the proper decoding and timing functions. It is responsible for selecting the memory configuration (Refer to Chapter 3, Section 2). The MIOC has 22 input signals, 16 output signals, power and ground.

2.1.4 ROM Circuitry

Room is provided on the Memory and I/O Board for up to 40K of ROM. ROM selection is controlled by a decoder circuit which is driven by A13, $\overline{\text{BOOTROMCS}}$ and $\overline{\text{EOS ENABLE}}$. The Memory and I/O Board ROM circuit contains EOS (Elementary Operating System) software.

2.1.5 Dynamic RAM Circuitry

The dynamic RAM circuit consists of eight 64K RAM chips arranged so that each represents one specific data bus bit. Information written to or read from RAM is controlled by the $\overline{\text{BWR}}$, $\overline{\text{RAS}}$ and $\overline{\text{CAS1}}$ signals. The latched Z80 address bus BA0 - BA15 (or BA0 - BA6, RA7, BA8 - BA15) is provided along with MUX from the MIOC to the two data selector multiplexers, which output MA0 - MA7 (or RA7) to the DRAM address bus. The Z80 provides a 7-bit refresh address after each instruction fetch. The MIOC generates an eighth bit for 256-refresh cycle dynamic RAMS. See Appendix 2, Adam Emulation Considerations for further information.

2.1.6 AdamNet Interface Circuitry

A quad comparator circuit provides data to and from the Master 6801 microcomputer via a half-duplex 62.5 kilobaud

serial network called AdamNET. The comparator also can reset all the devices on AdamNET via MIOC control. AdamNET links the tape drive, printer and keyboard to the Master 6801. Each of these peripherals has a 6801 and a quad comparator circuit that control AdamNET. Besides the data signal and reset signal, ground and power are provided as part of the AdamNET bus.

2.1.7 Card Edge Expansion Connectors

Three card edge connectors are provided for future development. Refer to Subsection 2.1.9 for pin connections.

2.1.7a Connector #1

This connector is soldered to the Memory and I/O Board, and is labelled J7.

2.1.7b Connector #2

This connector is designed for expansion ROM and I/O devices and is soldered to the Memory and I/O Board. It is labelled J6.

2.1.7c Connector #3

This connector allows for expansion RAM and/or ROM up to 64K bytes, and is labelled J5.

2.1.8 Expansion Port

The expansion port is connected to the Memory and I/O Board at P1.

Pin	Type	Refer To Table
1	Ground	
2	Ground	
3	BD3 Tristate, I/O	1, 2
4	BA14 Tristate output	1, 2
5	Y2 LS138 decoder output	
6	Y1 LS138 decoder output	
7	$\overline{\text{HALT}}$ input	1, 2
8	$\overline{\text{BWR}}$ Tristate output	1, 2
9	$\overline{\text{NMI}}$ input/output	1, 2
10	$\overline{\text{SPINNER INT DISABLE}}$ input	1
11	$\overline{\text{BUSRQ}}$ input	1
12	$\overline{\text{BD1}}$ Tristate, I/O	1, 2
13	Z80 Reset input	1, 2
14	$\overline{\text{BD0}}$ Tristate, I/O	1, 2
15	$\overline{\text{BM1}}$ Tristate output	1, 2
16	BD7 Tristate, I/O	1, 2
17	BD6 Tristate, I/O	1, 2
18	BA1 Tristate output	1, 2
19	BD4 Tristate, I/O	1, 2
20	BA2 Tristate	1, 2
21	BA4 Tristate output	1, 2
22	BA13 Tristate output	1, 2
23	BA5 Tristate output	1, 2
24	BA6 Tristate output	1, 2
25	BA7 Tristate output	1, 2
26	BA8 Tristate output	1, 2
27	BA9 Tristate output	1, 2
28	$\overline{\text{BA10}}$ Tristate output	1, 2
29	$\overline{\text{AUX DECODE 1}}$ input	1
30	$\overline{\text{AUX DECODE 2}}$ input	1
31	Audio input	
32	Video input enable + 9VDC	
33	NTSC Composite video input, 6VDC, 1.5 VAC	
34	$\overline{\text{GAME MODE RESET}}$ output	
35	Sound chip 76489 disable, 0 Volts DC	
36	Not in use	
37	BA11 Tristate output	1, 2
38	BA12 Tristate output	1, 2
39	VDP Sync/Reset input	1
40	$\overline{\text{BIORQ}}$ Tristate output	
41	Not used	
42	Not used	1
43	BA15 Tristate output	1, 2
44	BA3 Tristate output	1, 2
45	B03.58 MHz clock	
46	BD2 Tristate, I/O	1, 2
47	BA0 Tristate output	1, 2
48	$\overline{\text{BD5}}$ Tristate, I/O	1, 2
49	$\overline{\text{BRFSH}}$ Tristate output	
50	$\overline{\text{WAIT}}$ input	1, 2
51	$\overline{\text{INT}}$ input	1, 2
52	$\overline{\text{BUSAK}}$ output	1, 2
53	$\overline{\text{BRD}}$ Tristate output	1, 2
54	$\overline{\text{BMREQ}}$ Tristate output	1
55	$\overline{\text{IORQ}}$ output	1, 2
56	AUDIO 76489 RDY output	
57	+12V	
58	+5V	
59	+5V	
60	-5V	

$\overline{X}$ - Denotes active low

TABLE 1: DC CHARACTERISTICS

Symbol	Parameter	Min	Typ	Max	Units	Test Conditions
V_{IL}	Input low voltage	-0.3		0.8	V	
V_{IH}	Input high voltage	2.0		V_{cc}	V	
V_{OL}	Output low voltage			0.4	V	I_{OL} = 1.8mA
V_{OH}	Output high voltage	2.4			V	I_{OH} = 250uA
ILI	Input leakage current			±10	uA	V_{IN} = 0 to V_{cc}
I_{LO}	Tri-state output Leakage current in float			±10	uA	V_{OUT} = 0.4V to V_{cc}

TABLE 2: TIMING REFERENCE TABLE

[ ]* See notes at end of table

SIGNAL	SYMBOL	PARAMETER	MIN (ns)	MAX (ns)
A_{0-15}	$t_{D(AD)}$	Address output delay		110
	$t_{F(AD)}$	Delay to float		90
	t_{acm}	Address stable prior to $\overline{MREQ}$ (memory cycle)	[1]*	
	t_{aci}	Address stable prior to $\overline{IORQ}$, $\overline{RD}$ or $\overline{WR}$ (I/O cycle)	[2]*	
	t_{ca}	Address stable from $\overline{RD}$, $\overline{WR}$ $\overline{IORQ}$ or $\overline{MREQ}$	[3]*	
	t_{caf}	Address stable from $\overline{RD}$ or $\overline{WR}$ during float	[4]*	
D_{0-7}	$t_{D(D)}$	Data output delay		150
	$t_{F(D)}$	Delay to float during write cycle		90
	$t_{S\overline{\Phi}(D)}$	Data setup time to rising edge of clock during M1 cycle	35	
	$t_{S\overline{\Phi}(D)}$	Data setup time to falling edge at clock during M2 to M5	50	
	t_{dcm}	Data stable prior to $\overline{WR}$ (memory cycle)	[5]*	
	t_{dci}	Data stable prior to $\overline{WR}$ (I/O cycle)	[6]*	
	t_{dcf}	Data stable from $\overline{WR}$	[7]*	
	t_H	Input hold time	0	
$\overline{MREQ}$	$t_{DL\overline{\Phi}(MR)}$	MREQ delay from falling edge of clock, $\overline{MREQ}$ low	20	85
	$t_{DH\overline{\Phi}(MR)}$	MREQ delay from rising edge of clock, $\overline{MREQ}$ high		85
	$t_{DH\overline{\Phi}(MR)}$	MREQ delay from falling edge of clock $\overline{MREQ}$ high		85
	$t_{w(\overline{MRL})}$	Pulse width, $\overline{MREQ}$ low	[8]*	
	$t_{w(\overline{MRH})}$	Pulse width, $\overline{MREQ}$ high	[9]*	
$\overline{IORQ}$	$t_{DL\overline{\Phi}(IR)}$	$\overline{IORQ}$ delay from rising edge of clock $\overline{IORQ}$ low		75
	$t_{DL\overline{\Phi}(IR)}$	IORQ delay from falling edge of clock $\overline{IORQ}$ low		85
	$t_{DH\overline{\Phi}(IR)}$	IORQ delay from rising edge of clock, $\overline{IORQ}$ high		85
	$t_{DH\overline{\Phi}(IR)}$	IORQ delay from falling edge of clock, $\overline{IORQ}$ high		85

TABLE 2: TIMING REFERENCE TABLE (Cont'd)

[ ]* See notes at end of table

SIGNAL	SYMBOL	PARAMETER	MIN (ns)	MAX (ns)
$\overline{RD}$	$t_{DL\Phi\downarrow(RD)}$	$\overline{RD}$ delay from rising edge of clock, $\overline{RD}$ low		85
	$t_{DL\Phi\downarrow(RD)}$	$\overline{RD}$ delay from falling edge of clock, $\overline{RD}$ low		95
	$t_{DH\Phi\uparrow(RD)}$	$\overline{RD}$ delay from rising edge of clock, $\overline{RD}$ high	15	85
	$t_{DH\Phi\downarrow(BD)}$	$\overline{RD}$ delay from falling edge of clock, $\overline{RD}$ high		85
$\overline{WR}$	$t_{DL\Phi\downarrow(WR)}$	$\overline{WR}$ delay from rising edge of clock, $\overline{WR}$ low		65
	$t_{DL\Phi\downarrow(WR)}$	$\overline{WR}$ delay from falling edge of clock, $\overline{WR}$ low		80
	$t_{DH\Phi\uparrow(WR)}$	$\overline{WR}$ delay from falling edge of clock, $\overline{WR}$ high		80
	$t_{w(\overline{WRL})}$	Pulse width, $\overline{WR}$ low	[10]*	
$\overline{M1}$	$t_{DL(M1)}$	$\overline{M1}$ delay from rising edge of clock $\overline{M1}$ low		100
	$t_{DH(M1)}$	$\overline{M1}$ delay from rising edge of clock M1 high		100
$\overline{RFSH}$	$t_{DL(RF)}$	$\overline{RFSH}$ delay from rising edge of clock, $\overline{RFSH}$ low		130
	$t_{DH(RF)}$	$\overline{RFSH}$ delay from rising edge of clock, $\overline{RFSH}$ high		120
$\overline{WAIT}$	$t_{S(WT)}$	$\overline{WAIT}$ setup time to falling edge of clock	70	
$\overline{HALT}$	$t_{D(HT)}$	$\overline{HALT}$ delay time from falling edge of clock		300
$\overline{INT}$	$t_{s(IT)}$	$\overline{INT}$ setup time to rising edge of clock	80	

TABLE 2: TIMING REFERENCE TABLE (Cont)

[ ]* See notes at end of table

SIGNAL	SYMBOL	PARAMETER	MIN (ns)	MAX (ns)
$\overline{NMI}$	$t_{w(NMI)}$	Pulse width, $\overline{NMI}$ low	80	
$\overline{BUSRQ}$	$t_{S(BQ)}$	$\overline{BUSRQ}$ setup time to rising edge of clock	50	
$\overline{BUSAK}$	$t_{DL(BA)}$	$\overline{BUSAK}$ delay from rising edge of clock, $\overline{BUSAK}$ low		100
	$t_{DH(BA)}$	$\overline{BUSAK}$ delay from falling edge of clock, $\overline{BUSAK}$ high		100
$\overline{RESET}$	$t_{s(RS)}$	$\overline{RESET}$ setup time to rising edge of clock	60	
	$t_{F(C)}$	Delay to/from float ($\overline{MREQ}$, $\overline{IORQ}$, $\overline{RD}$, and $\overline{WR}$		80
	t_{mr}	$\overline{M1}$ stable prior to $\overline{IORQ}$ (interrupt Ack.)	[11]*	

Timing Reference Table Notes

[1] $t_{acm} = t_w(\emptyset H) + t_f - 65$
[2] $t_{aci} = t_c - 70$
[3] $t_{ca} = t_w(\emptyset L) + t_r - 50$
[4] $t_{caf} = t_w(\emptyset L) + t_r - 45$
[5] $t_{dcm} = t_c - 170$
[6] $t_{dci} = t_w(\emptyset L) + t_r - 170$
[7] $t_{cdf} = t_w(\emptyset L) + t_r - 70$
[8] $t_w(\overline{MRL}) = t_c - 30$
[9] $t_w(\overline{MRH}) = t_w(\emptyset H) + t_f - 20$
[10] $t_w(WRL) = t_c - 30$
[11] $t_{mr} = 2t_c + t_w(\emptyset H) + t_f - 65$

t_c = clock period: 279.36 ns $\pm$ .01
$t_{w(\emptyset H)}$= clock pulse width, clock High = 120 ns min
$t_{w(\emptyset L)}$ = clock pulse width, clock Low = 120 ns min
t_f = clock fall time = 15 ns max
t_r = clock rise time = 15 ns max

2.1.9 Interconnects

2.1.9a Memory and I/O Board/CPU Board

The Memory and I/O Board is connected to the CPU Board at J1, with two 30-pin ribbon cables and a dual 30-pin card edge connector.

Signal	Description
BD0-BD7	8 bidirectional data lines. BD0 is least significant, BD7 is most significant.
BA0-BA15	16 address lines to Memory and I/O Board. BA0 is least significant, BA15 is most significant.
$\overline{\text{BWR}}$	Output of Z80 to Memory and I/O Board; write strobe used to output data during an I/O or memory operation. Indicates a write operation.
$\overline{\text{BRD}}$	Output of Z80 to Memory and I/O Board; read strobe used to clock data into the Z80 during an I/O or memory operation.
$\overline{\text{BMREQ}}$	Output of Z80 to Memory and I/O Board; indicates present read or write operation is directed to memory or memory-mapped devices.
$\overline{\text{IORQ}}$ $\overline{\text{BIORQ}}$	Same as $\overline{\text{BMREQ}}$, but indicates an I/O operation instead of memory or memory-mapped devices
$\overline{\text{BRFSH}}$	Output of Z80 to Memory and I/O Board; indicates BA0-BA6 contain a row address for the required dynamic memory refresh. (An eighth row address bit is generated by the MIOC 'RA7'.)
$\overline{\text{RST}}$	Generated by the MIOC as a result of either a game $\overline{\text{CVRST}}$ or computer $\overline{\text{PBRST}}$ reset. It connects to and resets the Colecovision or CPU Board.
Bϕ	System clock generated on Colecovision or CPU Boards. Line connects to Memory and I/O Board.

$\overline{\text{WAIT}}$	Used to insert extra clock cycles into Z80 timing during opcode fetch cycles and when accessing slow memory or I/O. Excessive use of $\overline{\text{WAIT}}$ causes inadequate dynamic RAM refresh.
$\overline{\text{ADDRBUFEN}}$	An active low signal enables the address and control signal buffers between the Colecovision or CPU Board, and the Memory and I/O Board. The control signals are $\overline{\text{BRD}}$, $\overline{\text{BWR}}$, $\overline{\text{BRFSH}}$, $\overline{\text{BMREQ}}$, $\overline{\text{BM1}}$, and $\overline{\text{BIORQ}}$. A high level disables these signals from the Z80, and allows them to go tristate (high-impedance). This occurs during a DMA cycle where another device needs to access memory or devices on the Memory and I/O Board. See $\overline{\text{BUSRQ}}$ and $\overline{\text{BUSAK}}$.
$\overline{\text{245EN}}$	Same as ADDRBUFEN except $\overline{\text{245EN}}$ controls the buffer for BD0 through BD7 data lines to CPU or Colecovision buffer board.
$\overline{\text{BUSRQ}}$(unbuffered) $\overline{\text{BUSAK}}$(buffered)	$\overline{\text{BUSRQ}}$ is generated by the MIOC as the result of a DMA request. The $\overline{\text{BUSRQ}}$ signal requests that the Z80 relinquish the address and data busses and certain control signals at the end of its current cycle. After receiving the $\overline{\text{BUSRQ}}$ the Z80 responds with a $\overline{\text{BUSAK}}$ signal to indicate it has relinquished the bus. The Z80 remains in an inactive state until the controlling device removes the $\overline{\text{BUSRQ}}$ signal. The $\overline{\text{BUSRQ}}$ line connects to the Colecovision orCPU Board. Generally, only the master 6801 may assert a $\overline{\text{BUSRQ}}$.
$\overline{\text{BM1}}$	Output of Z80 from CPU or Coleco-vision Board; indicates the present memory cycle is an opcode fetch (start of next instruction).
$\overline{\text{CVRST}}$	This signal generates an $\overline{\text{RST}}$ to the Z80 processor. Also reset are the MIOC and master 6801. $\overline{\text{CVRST}}$ initializes the MIOC memory map such that addresses from 0-1FFFH enable the OS-7 ROM; 2000H through 7FFFH enable RAM1; and 8000H through FFFFH enables the game cartridge.
$\overline{\text{AUXDECODE1}}$	Generated by Memory and I/O Board. Selects or deselects the OS-7 ROM.

$\overline{\text{INT}}$	Active low, this signal is an input to the Z80 and results in a maskable interrupt which directs the Z80 to respond to some external event.
$\overline{\text{SPINDIS}}$	Allows disabling of spinner interrupts by the hand controllers. Active low.
Audio Out Audio In AUX VID VID GATE CLK, $\overline{\text{RSTDIS}}$ $\overline{\text{SEL4}}$, $\overline{\text{SEL2}}$ $\overline{\text{HALT}}$, $\overline{\text{NMI}}$ $\overline{\text{AUXDECODE2}}$ $\overline{\text{VIDRST}}$	These signals are not used on the Memory and I/O Board but are made available at the expansion connector.

2.1.9b Interconnects for Connector #1 at J7

BD0-BD7	8 bidirectional data lines. BD0 is least significant, BD7 is most significant.
BA0-BA7	Address lines to Memory and I/O Board. BA0 is least significant, BA7 is most significant.
$\overline{\text{BWR}}$	Output of Z80 to Memory and I/O Board; write strobe used to output data during an I/O or memory operation. Indicates a write operation.
$\overline{\text{BRD}}$	Output of Z80 to Memory and I/O Board; read strobe used to clock data into the Z80 during an I/O or memory operation.
$\overline{\text{IORQ}}$ $\overline{\text{BIORQ}}$	Same as $\overline{\text{BMREQ}}$, but indicates an I/O operation instead of memory or memory-mapped devices.
$\overline{\text{BM1}}$	Output of Z80 from CPU or Coleco-vision Board; indicates the present memory cycle is an opcode fetch (start of next instruction).
$\overline{\text{INT}}$	Active low, this signal is an input to the Z80 and results in a maskable interrupt which directs the Z80 to respond to some external event.

2.1.9c Interconnects for Connector #2 at J6

BD0-BD7	8 bidirectional data lines. BD0 is least significant, BD7 is most significant.
BA0-BA15	16 address lines to Memory and I/O Board. BA0 is least significant, BA15 is most signifi cant.
$\overline{\text{BWR}}$	Output of Z80 to Memory and I/O Board; write strobe used to output data during an I/O or memory operation. Indicates a write operation.
$\overline{\text{BRD}}$	Output of Z80 to Memory and I/O Board; read strobe used to clock data into the Z80 during an I/O or memory operation.
$\overline{\text{BMREQ}}$	Output of Z80 to Memory and I/O Board; indicates present read or write operation is

directed to memory or memory-mapped devices.

$\overline{\text{IORQ}}$ $\overline{\text{BIORQ}}$	Same as $\overline{\text{BMREQ}}$, but indicates an I/O operation instead of memory or memory-mapped devices. $\overline{\text{IORQ}}$ is unbuffered; $\overline{\text{BIORQ}}$ is buffered.
$\overline{\text{BM1}}$	Output of Z80 from CPU or Coleco-vision Board; indicates the present memory cycle is an opcode fetch (start of next instruction).
$\overline{\text{INT}}$	Active low, this signal is an input to the Z80 and results in a maskable interrupt which directs the Z80 to respond to some external event.
AUDIO IN	

2.1.9d Interconnects for Connector #3 at J5

BD0-BD7	8 bidirectional data lines. BD0 is least significant, BD7 is most significant.
BA0-BA15	Address lines to Memory and I/O Board. BA0 is least significant, BA15 is most significant. RA7 is substituted for BA7.
$\overline{\text{BWR}}$	Output of Z80 to Memory and I/O Board; write strobe used to output data during an I/O or memory operation. Indicates a write operation.
$\overline{\text{BRD}}$	Output of Z80 to Memory and I/O Board; read strobe used to clock data into the Z80 during an I/O or memory operation.

2.1.9e Other Memory and I/O Board Connections

J2 and J8 AdamNet Connections - The following signals are found on the AdamNet connectors for keyboard and expansion devices.

Data - 62.5K bps serial 'bidirectional' line for data transmission reception by network devices.

Reset - hardware network reset

+5V

Signal Ground

J9 Power Supply/Printer Connector - In addition to containing the signals found on J2 and J8, the necessary power supply voltages of +12V Logic, +12V Inductive, and -5V connect here.

J10 and J12 Data Drive Connectors - For a detailed description of the signals found on the data drive connectors, refer to Subsection 2.3.5.

J1 Cartridge Connector

Pin	Type	Pin	Type	Pin	Type	Pin	Type	Pin	Type
1	D2	7	A0	13	RF ground	19	A13	25	A7
2	CS3*	8	D5	14	A11	20	A14	26	A9
3	D1	9	A1	15	A3	21	A5	27	CS4*
4	D3	10	D6	16	A10	22	CS2*	28	A8
5	D0	11	A2	17	A4	23	A6		
6	D4	12	D7	18	CS1*	24	A12		

30 +5V Typical available current 0.2A
29 Digital Ground

*LS138 Decoder output. Refer to Table 3.

TABLE 3: CARTRIDGE INTERFACE PARAMETERS

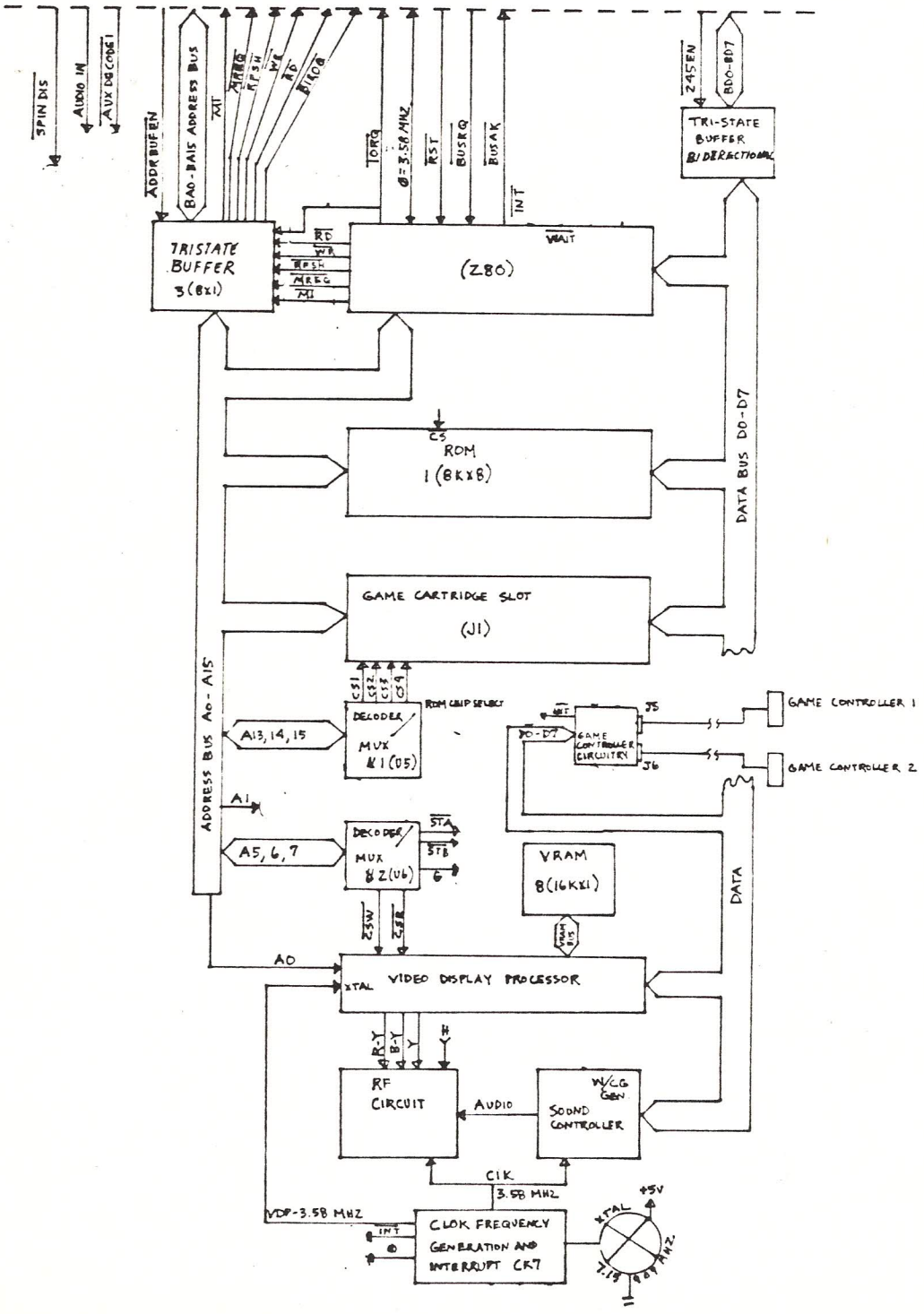
Symbol	Parameter	Conditions		Min Typ Max	Units
V_{OH}	High level output voltage	V_{cc} = Min, V_{IH} = 2V V_{IL} = V_{IL} Max, I_{OH} = - 400 uA		2.7 3.4	V
V_{OL}	Low level output voltage	V_{cc} = Min, V_{IH} = 2V V_{IL} = V_{IL} Max	I_{OL} = 8 mA	0.35 0.5	V
			I_{OL} = 4 mA	0.25 0.4	
V_{IH}	High level input voltage			2	V
V_{IL}	Low level input voltage			0.8	V

2.2 THE CPU BOARD

2.2.1 Theory of Operation

The CPU Board, located in the console of the Adam computer system, consists of six major units: The Z80 Central Processing Unit (CPU), a Video Processor, an Audio Generator, the RF Modulator, Clock Generation and the Game Controller Section. The Z80 is the CPU of the entire computer system all other microprocessors are slaves.

FIGURE 2-4: CPU BOARD BLOCK DIAGRAM



2.2.2 Z80 Microprocessor

The Z80 CPU, which consists of a Z80A microprocessor and a clock circuit for synchronization, has control of the Adam computer system. The Z80 configures the memory map and can switch banks of memory. Refer to Chapter 3, Section 2 for details on the memory configuration.

2.2.3 ROM Circuitry

The CPU Board includes an 8K operating system ROM (OS_7) and a connector for up to 32K of cartridge ROM.

2.2.4 Video Display Processor (VDP)

The Video Display Processor, a Texas Instruments (TI) 9928, generates all video, control and synchronization signals and controls the storage, retrieval and refresh of display data in a dynamic memory, VRAM. The 9928 uses a table-driven architecture that allows the programmer to control every pixel in the visual display area, and to define and control 32 "sprites." Sprites may be placed anywhere on the display and moved at will.

The VDP has three major interfaces: CPU, RF modulator, and VRAM. The VDP is addressable in data mode (used when VRAM is being written or read) and register mode (used when control information is being written to and read from one of the VDP's internal registers). The addresses of the ports in the CPU I/O address space are as follows:

Data Port ...0BEH
Register Port ...0BFH

The video RAM circuit consists of 8 (16384 x 1) RAM integrated circuits. The contents of VRAM define the TV image. A0, $\overline{CSW}$ and $\overline{CSR}$ are CPU-controlled input signals to the VDP that control when the data is written to or read from VRAM. The VDP output signals $\overline{R/W}$, $\overline{CAS}$ and $\overline{RAS}$ control the RAM operation.

Data can be transmitted to or from the CPU over the data bus, depending on the state of the Chip Select Write ($\overline{CSW}$) and Chip Select Read ($\overline{CSR}$) control lines. When $\overline{CSW}$ is low, data is transmitted from the CPU to the Video Display Processor. When $\overline{CSR}$ is low, data is transmitted from the Video Display Processor to the CPU. $\overline{CSR}$ and $\overline{CSW}$ should not be simultaneously low.

Another control line, address line A0, determines where the VDP retrieves or sends data. If A0 is in a high state, the

data is stored into, or retrieved from an internal register. The register used is determined by the data. If A0 is in a low state, the data is stored into or retrieved from the VRAM.

Refer to the Texas Instruments TMS9918A/TMS9928A/TMS9929A Video Display Processors Data Manual for further information.

2.2.5 Sound Generator

The system uses a TI 76489 (6496) sound generator controller to produce sounds. The chip contains three programmable tone generators, a programmable white-noise generator, and programmable attenuation for each of the channels. The chip is addressed through a single write-only port at location OFFH. Wait-request hardware has been included in the system because the sound chip is a slow peripheral requiring data lines to be stable for a relatively long time while it is receiving data.

2.2.6 RF Circuitry

The RF modulator uses the 1889 chip to interface audio, color difference, and luminance signals to the antenna terminals of a TV receiver. It consists of two VHF channels, 3 or 4, selectable by a slide switch with determined LC tank circuits. The Chroma subcarrier is derived from the 3.58 MHz system clock to ensure accuracy and stability. The sound oscillator's frequency modulator is achieved by using a 4.5 MHz tank circuit and deviating the center frequency via a varactor diode. Due to the incompatible signal level between the VDP 9928 and the 1889, a DC restoration circuit ensures the DC level of the video signal.

The $\overline{R-Y}$, $\overline{B-Y}$, and Y signals from the VDP, along with the 3.58 MHz clock and the audio signal from the SN76489 (6496), are provided to the RF modulator to produce the composite video output.

2.2.7 Game Controller Circuitry

The two game controllers are connected to the CPU Board via two "D" type connectors. Each controller is accessed by the system through its own port. See CONT-SCAN in the OS_7 Source Code Listing for details.

For each controller, 18 switches are read on a single 8-bit port. Therefore, once a port has been read, some decoding is required to determine which switches have been depressed.

Two spinner switches that are not wired in the controller are used in some games. To ensure that the spinner switch closures are processed as soon as they happen, they are connected to the CPU maskable interrupt, and the cartridge software determines which switch causes the interrupt.

Controller Connector Pin Out

Pin	Type	Comments
1	Indirect D0 input	Refer to Table 1
2	Indirect D2 input	Refer to Table 1
3	Indirect D3 input	Refer to Table 1
4	Indirect D1 input	Refer to Table 1
5	Strobe signal output, Common 1	
6	Indirect D6 input	Refer to Table 1
7	Indirect D5 input	Refer to Table 1
8	Strobe signal output, Common 0	
9	Indirect INT input	

Strobe signal: typical 350 micro sec pulse width, -0.7V Low, +2.8V high typ.

For further information on the game controllers, refer to Chapter 2, Section 5.

2.2.8 Clock Generation

The system clock is a 3.58 MHz square wave generated by dividing the 7.1 MHz clock by two. The video chip clock (10.7 MHz) drives the Video Display Processor. The video chip clock is obtained from the third multiple, high Q tuned tank circuit on the 3.58 MHz system clock. The 7.1 MHz clock is generated by a crystal controlled oscillator. The output of the oscillator circuit is buffered and divided by two to provide a 50% duty cycle wave form.

2.2.9 Interconnects

The CPU Game Board and the Memory and I/O Board connect via two 30-pin ribbon cables and a dual 30-pin card edge connector, making a pin-for-pin connection between J1 on the Memory and I/O Board and J2 on the CPU Board. Refer to Subsection 2.1.9.

2.3 DATA PACK DRIVE MODULE

2.3.1 Theory of Operation

The data drive assembly provides for two drives: one is included with the system, the other is optional. The data drive is a computer-controlled, digital cassette drive.

The components of the data drive subsystem are located in two places: The Memory and I/O Board contains the tape drive 6801 microcomputer, a quad comparator and RAM. The Read/Write and Servo Boards are located in the data drive assembly.

The data drive 6801 controls the direction of the tape, tape speed, stop, track selection, and the Read/Write operation. In addition, the data drive 6801 monitors the presence of a data pack and transmits and receives data through AdamNet.

The comparator interfaces the data drive 6801 to AdamNet. The RAM circuitry consists of two 1024 x 4 ROM integrated circuits, connected in parallel to provide an 8-bit data bus.

Two printed circuit boards, the Servo Board and the Read/Write Board are located in the data drive assembly.

2.3.2 The Servo Board

The Servo Board controls the direction and speed of the data drive by:

Controlling the "take-up" motor which pulls tape in the direction of motion (forward or reverse).

Controlling the "supply" motor which applies a slight pull or drag in the direction opposite to tape motion. This function maintains a stable tape motion.

Maintaining a constant tape velocity across the head at any position, from the beginning to the end of the tape.

Providing two different tape speeds; 20 inches per second (slow), and 80 inches per second (fast). Tape speed is controlled by the data drive 6801.

Providing a brake function that allows the data drive 6801 to stop tape motion in milliseconds. (This function prevents the tape from coasting to a stop.)

Keeping the tape in tension when the tape is not in motion, preventing slack in the tape.

Providing a signal to the data drive 6801 indicating the status of tape motion.

Providing a signal to the data drive 6801 indicating whether or not a data pack has been properly placed in the data drive.

2.3.3 The Read/Write Board

The Read/Write Board records digital data encoded in bi-phase mark format on two separate tracks on the tape. This board also plays back the data recorded on the two tracks, with data output in the same format as recorded. The data drive 6801 selects the tracks.

The bi-phase mark technique embeds the clock in the data line. When data is returned from the data drive to the data drive 6801, the data line is coded back to the standard binary format.

A "cassette-in-place" switch located on the data drive chassis lets the Servo Board know when the data pack is in place and ready for use. An optical encoding wheel interacts with the Servo Board and the tape for drive speed control.

2.3.4 Data Pack Specifications

The magnetic tape in the data pack is standard two-track digital recording tape, 300 feet in length by .15 inches in width.

Effective data transfer rate	1.4K bytes per second
Tape speed	
Normal	20 inches per second
Fast forward/rewind	80 inches per second
Tape capacity	256K bytes
	Two tracks, 128 blocks per track
	1 block = 1K

2.3.5 I/O Signals between Memory and I/O Board and Data Drive

Signal Name	Mem/I/O Board	R/W I/O	Description
(input) BRAKE*	J10-1	E26	Brakes tape motion. Logic 1 (active high) applies brake. This signal is passed from the Read/Write (RW) Board to the Servo Board at point E6.
(input) GO REV	J10-2	E25	Commands reverse direction of tape motion when at Logic 0 (active low). This signal is passed from R/W Board to Servo Board at point E8.
(input) GO FWD	J10-3	E27	Commands forward direction of tape motion when at Logic 0 (active low). This signal is passed from R/W Board to Servo Board at point E8.
(input) STOP	J10-4	E28	Prevents tape motion and latches data drive output to Logic 1 when at Logic 1 (active high). Enables data drive output and tape motion when at Logic 0. This signal is used in circuits on both boards. It is passed from R/W Board to Servo Board at point E9.
(input) SPEED SELECT	J10-5	E29	Selects speed of tape motion; Logic 0 = 20 ips (slow speed), Logic 1 = 80 ips (fast speed). This signal is passed from R/W Board to Servo Board at E10.
GND	J10-6	E30	Return path for all logic and analog signals. Connected from R/W Board to Servo Board at point E19.

2.3.5 I/O Signals between Memory/I/O Board and Data Drive (continued)

Signal Name	Mem/I/O Board	R/W I/O	Description
(output) MSENSE	J10-7	E31	Provides sense of tape motion status for tape drive 6801 (active high). When Logic 1, tape is properly in motion. When Logic 0, tape is not moving due to stop/braking action or malfunction. This signal is passed between R/W Board and Servo Board at point E12.
(input) +12VI	J10-8	E32	+12V Inductive Power Supply line, used to power motor circuitry. Passed from R/W to Servo circuit at point E12.
(output) CIP	J10-9	E33	Indicates to tape drive 6801 that a data pack has been properly inserted in drive when Logic 0 (active low). Passed between R/W and Servo Boards at point E14.
(input) DATA IN	J11-1	E17	Data input to drive from tape drive 6801. Data is encoded in bi-phase mark format. Each bit cell is 70 micro-seconds in duration. A Logic 1 is denoted by a flux change in the bit cell. A Logic 0 is denoted by no flux change in the bit cell. This data is input to the drive in a serial stream.
(input) TRACK A/$\overline{B}$	J11-2	E18	Selects recording track for read or write operation. Logic 1 selects Track A; Logic 0 selects Track B.
GND	J11-3	E19	Return path for all analog and logic signals.

2.3.5 I/O Signals between Memory/I/O Board and Data Drive (continued)

Signal Name	Mem/I/O Board	R/W I/O	Description
(input) +5V	J11-4	E20	+5V is passed to Servo Board at point E3.
(output) DATA OUT	J11-5	E21	Data output from drive to tape drive 6801. Data is encoded in bi-phase mark format as described in DATA IN signal. Jitter in signal is specified at 4% maximum, peak shift at 5% maximum.
(input) +12VL	J11-6	E22	+12V is passed from R/W to Servo Board at point E15.
(input) $\overline{\text{WRENABLE}}$	J11-7	E23	Selects write mode (Logic 0) or read mode (Logic 1) of R/W circuit operation (active low).
-	J11-8	E24	No connection.

2.4 Differences of Expansion Module #3

Expansion Module #3 is designed for the consumer who owns ColecoVision. It consists of the Memory Console, the keyboard, the printer, and various cords and cables to connect the components. The Memory Console attaches to the ColecoVision Console. The consumer provides his own TV. The major difference between Expansion Module #3 and the complete Adam Home Computer System is in the Memory Console. The equivalent of the CPU Board is housed in the ColecoVision Console, not in the Memory Console. Expansion Module #3 does not provide composite video output; therefore a monitor cannot be used.

Expansion Module #3 is not packaged with "joystick" game controllers or the antenna switch box, since these items come with ColecoVision.

The ColecoVision Board and the Memory and I/O Board connect via two 30-pin ribbon cables, a dual 30-pin card edge connector and the Interconnect Board, making a connection between J1 on the Memory and I/O Board and the expansion port of the ColecoVision console. Many of the connections are made pin-for-pin. The exceptions are:

A0 - A15	These lines are buffered. The input to the buffer is from the ColecoVision and the tristate control of the buffer ($\overline{\text{ADDRBUFEN}}$) is from the Memory and I/O Board.
D0 -D7	These lines are buffered bidirectionally. The $\overline{\text{RD}}$ signal from the ColecoVision controls the direction (when active, data flows toward the ColecoVision) and the $\overline{\text{245EN}}$ signal controls the tristate function.
$\overline{\text{IORQ}}$	This line is connected directly between the two boards (pin 55) and is also buffered (controlled by $\overline{\text{ADDRBUFEN}}$) and connected to pin 40 of the Memory and I/O Board.
Ø'CLOCK	This line, pin 40 of the ColecoVision Board, is connected to pin 45 of the Memory and I/O Board.
Ø CLOCK	This line, pin 45 of the ColecoVision, is not connected.

$\overline{M1}$, $\overline{MREQ}$, $\overline{RFSH}$, $\overline{WR}$ $\overline{RD}$	These lines are buffered. The input to the buffer is from the ColecoVision, and the tristate control of the buffer ($\overline{ADDRBUFEN}$) is from the Memory and I/O Board.

3. THE KEYBOARD

3.1 Theory Of Operation

The keyboard is the major input device through which the user communicates with the system. The game controller joystick, buttons and keypad can also be used to input information. The keyboard consists of two major subsystems. The external subsystem is an array of keys much like that of an mechanical typewriter. The internal subsystem, located on the Keyboard Printed Circuit Board, includes the keyboard 6801 microcomputer and the AdamNet serial interface.

The keyboard contains 75 full travel keys, including special function keys. Some special function keys are labelled on the key top, for example, STORE/GET, DELETE, BACKSPACE. The function keys on the top row of the keyboard are smart keys, marked I through VI. Corresponding smart key labels shown on the video display identify their functions.

The keyboard 6801 determines which keys the user presses through the keyboard matrix. Every 5 or 8 milliseconds, the keyboard 6801 scans the matrix and stores the characters in a buffer.

The matrix consists of vertical columns which correspond to keyboard 6801 output lines and horizontal rows which correspond to keyboard 6801 input lines.

A debounce function determines if any of the keys registers a low signal; then that row is read horizontally. More than one row in a column is read if more than one key in that column is depressed. The ASCII code for the depressed key or keys is read back to the 6801. The keyboard 6801 compares the code with the code input from the previous scan. If it is the same, the information is recorded; it is different, the information is not recorded.

The keyboard 6801 responds to the following commands from the master 6801:

Reset - the keyboard 6801 erases the character buffer and resets shift lock to the unlocked state.

Send character - the keyboard 6801 sends one character via the RxD/TxD line to the master 6801.

3.2 Interconnects

The lines linking the keyboard 6801 to AdamNet are:

Signal ground
+5V (input)
Reset (input)
RxD/TxD (input/output)

4. THE PRINTER

4.1 Theory of Operation

The printer houses two printed circuit boards: the Printer Board and the Linear Power Supply Board. The Printer Board includes a 6801 microcomputer and parallel drivers that control the printer's electro-mechanical devices. The electro-mechanical devices include the daisy wheel motor, the carriage motor, the platen advance mechanism, the print solenoid, and the ribbon solenoid. The Linear Power Supply Board includes regulators, rectifiers, and a transformer. For more information on the power supply, refer to Chapter 2, Section 6.

4.2 The Printer Board

The printer 6801 communicates with the Master 6801 on the Memory and I/O Board via AdamNet to receive data to be printed, control the motions of the printer's mechanical parts, and ensure that the printer performs the optimum number of motions simultaneously.

Within the printer 6801 RAM is a 16-character buffer for data being sent to the printer over AdamNet. The buffer ensures that time is not lost between characters being printed, and maximizes printing speed.

The printer 6801 responds to some ASCII control codes including carriage return, line feed, backspace, escape, shift-out and shift-in. Shift-out causes the printer 6801 to reverse its left and right directions, allowing printing from right to left.

The printer 6801 controls the printer's electro-mechanical devices. It also ensures that lateral carriage motion, rotation of the daisy wheel and stepping of the platen can be activated simultaneously.

4.3 Interconnects

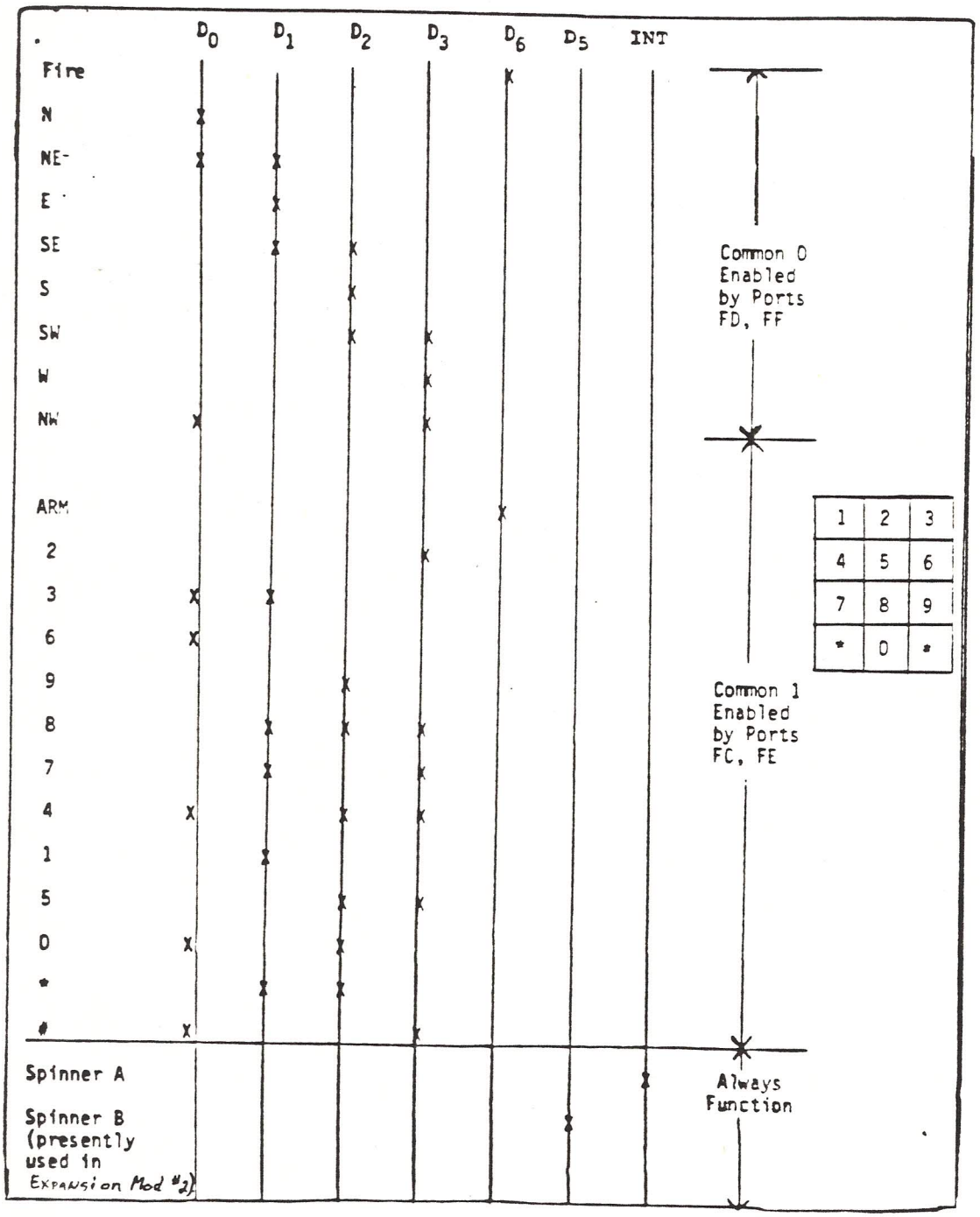
The lines linking the printer 6801 to AdamNet are:

Signal ground
+5V (input)
Reset (input)
RxD/TxD (input/output)

5. GAME CONTROLLERS

The game controller contains an 8-position joystick, two push buttons and a 12-key keypad. The information from a controller is read by the CPU on eight input lines through a single port. Once a port has been read, the input data must be decoded. See CONT_SCAN in the OS_7 Source Code Listing for details.

FIGURE 2-5: CONTROLLER CONFIGURATION



6. POWER SUPPLY

6.1 Power Supply Voltage

The power supply for the ADAM computer is located in the printer. The power supply converts the incoming line voltage (AC) to one 18V unregulated voltage that powers the ribbon solenoid and four low level, regulated DC voltages as follows:

+5v	Main source of power to the CPU
-5V	Supplies power to the CPU
+12VI	Supplies power to drive the inductive loads such as carriage motor, daisy wheel motor, print solenoid, platen motor and digital data drive.
+12VL	Supplies power to the system logic.

6.2 Excessive Current Output Protection

The power supply uses a variety of methods to protect against excessive current output.

The +5V and the +12VI are fused and use electronic foldback current limiting.

The +12VL is not fused but uses electronic foldback limiting.

The -5v uses conventional current limiting and thermal protection which halts the current when the regulator gets too hot.

The 18V unregulated uses the same fuse as the +12VI.

A thermal fuse in the power transformer protects against overcurrent at the transformer.

The AC line input may vary from 108VAC to 132VAC. The power supply ensures a constant and quiet source of DC power.

6.3 Printer/Memory Console Interface Cable

The printer/console interface cable consists of 7 insulated wires and one uninsulated drain wire.

Pin	Color	Voltage/Description
1	Brown	+12L VDC +.508V -.6V
2	Red	+12I VDC +.497V -.6V
3	Orange	+5.075 VDC +.079V -.255V
4	Yellow	-5.15VDC +.25V
5	Green	Ground
6	Blue	AdamNet
7	Violet	Reset
8	--	Drain
9	--	No wire

6.4 Power Supply Output to CPU (via Printer/Memory Console Interface Cable)

Voltage	Full Load Current
+5V	2.75A
-5V	0.2A
+12VI	0.6A
+12VL	0.3A

6.5 Power Supply Output to Printer

Voltage	Full Load Current
+5VL	0.25A
+12VI	1.95A
+18V (unreg)	1.0A