System Description

ColecoVision contains five basic parts: the Central Processing Unit (CPU), the video section, the audio section, the RF modulator and memory. The game has two handcontroller ports to input data and an expansion port which outputs the entire CPU bus, CPU control lines and selected inputs to the RF modulator, onto a 60 pin edge connector.

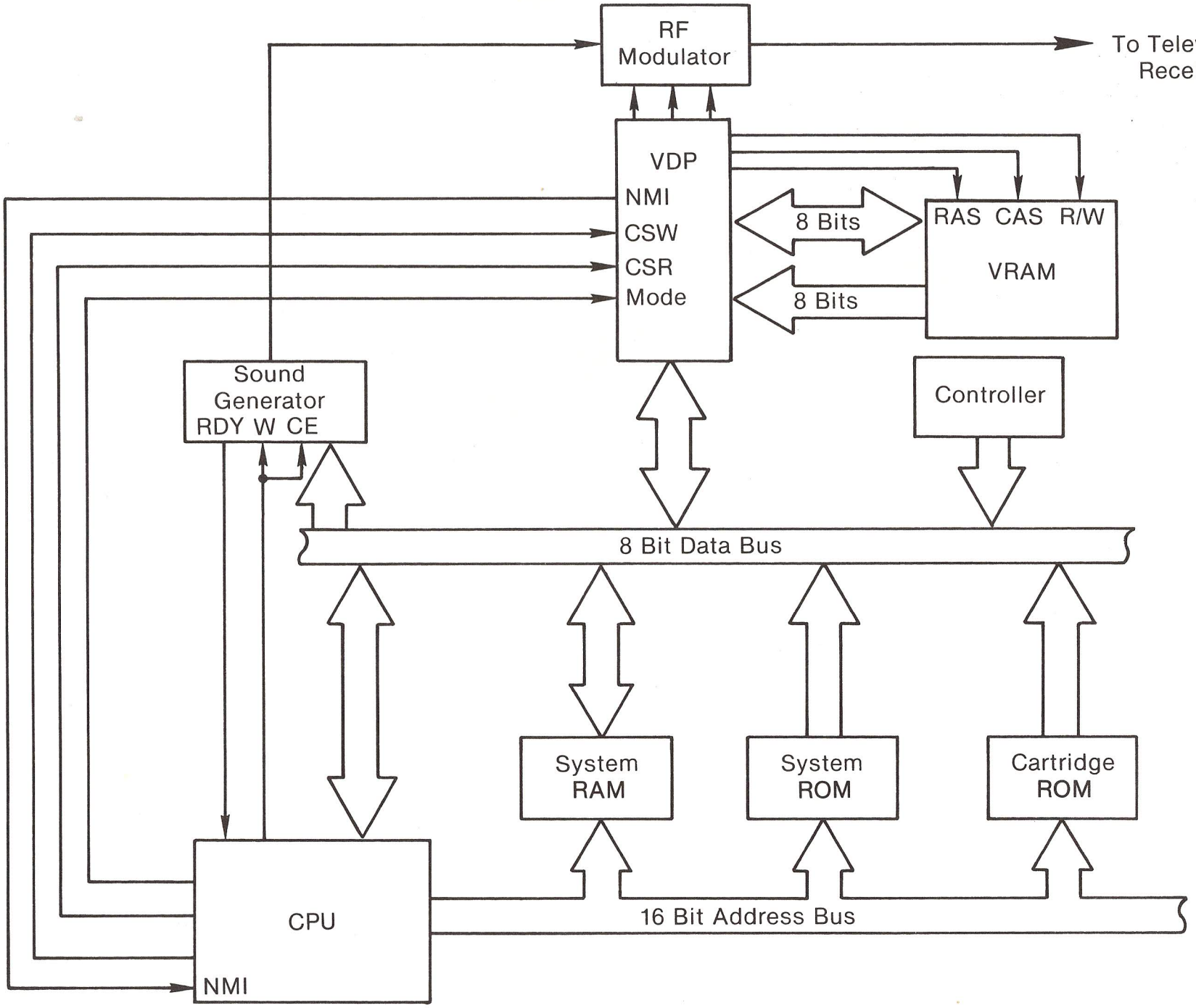
The CPU consists of a Z-80A microprocessor and support circuitry. The Z-80A has an eight bit data bus and a sixteen bit address bus. The support circuitry consists of a clock, reset circuitry and decoders.

The video section is made up of Texas Instrument's 9928 Video Display Processor (VDP) and eight Video RAM (VRAM). The VDP interfaces to the CPU via the eight bit data bus and four control signals, CSW, CSR, Mode (A0), and NMI. VRAM interfaces to the VDP via an eight bit bidirectional address/data bus, a unidirectional eight bit data bus and three control lines, RAS, CAS, and R/W. The video section outputs three signals to the RF modulator.

The audio section is basically the Texas Instrument's 76489 sound generator chip. The integrated circuit is on the eight bit CPU data bus and uses two other inputs to enable the chip along with the system clock for synchronization. The 76489 outputs a ready signal to the CPU when it has inputted the data on the data bus. It outputs audio to the RF modulator.

The RF modulator takes both the audio and video signals and outputs the RF modulated signal. Either channel 3 or 4 carrier frequencies can be selected by the channel selector switch.

ColecoVision uses three types of memory; System Read Only Memory (ROM), cartridge ROM, and Random Access Memory (RAM). The system ROM contains frequently used sub-routines. Cartridge ROM contains patterns and game rules for a particular game. RAM is used to store temporary information (scores, motion variables, etc.).


RF
Modulator
To Television
Receiver
VDP
NMI
CSW
CSR
Mode
8 Bits
8 Bits
RAS CAS R/W
VRAM
Sound
Generator
RDY W CE
Controller
8 Bit Data Bus
System
RAM
System
ROM
Cartridge
ROM
CPU
NMI
16 Bit Address Bus

CPU

The CPU is comprised of the Z-80A microprocessor, a clock circuit for synchronization and two decoders.

The clock circuit is made up of a 7.19 MHz crystal oscillator. This frequency is divided by two using a "D" flip-flop. This new frequency is the 3.58 MHz that is required for color burst.

The decoders are used to translate portions of the address bus to select the VDP, RAM, Cartridge ROM, System ROM and the grounds for the handcontrollers.

The Z-80A uses two busses, address and data. The Address Bus (A_0-A_{15}) provides the address for memory (up to 64K bytes unidirectional) data exchanges and for I/O device data exchanges. The A_0-A_{15} constitutes a 16 bit address bus. The Data Bus (D_0-D_7) consists of an 8 bit tri-state bidirectional data bus. It is used for data exchanges with memory and I/O devices.

In addition to the two busses the Z-80A has several control signals.

Machine Cycle One (M_1) indicates the current machine cycle is the OP code fetch cycle of an instruction execution. Output, active low.

Memory Request (MREQ) signal indicates the address bus holds a valid address for a memory read or memory write operation. Tri-state output, active low.

Input/Output Request (IORQ) signal indicates the lower half of the address bus holds a valid I/O address for an I/O read or write operation. An IORQ signal is also generated when an interrupt is being acknowledged to indicate that an interrupt response vector can be placed on the data bus. Tri-state output, active low.

Memory Read (RD) indicates the CPU wants to read data from memory or an I/O device. The addressed I/O device or memory should use this signal to gate data onto the CPU data bus. Tri-state output, active low.

Memory Write (WR) indicates the CPU data bus holds valid data to be stored in the addressed memory or I/O device. Tri-state output, active low.

Refresh (RFSH) indicates the lower seven bits of the address bus contain a refresh address for dynamic memories and the current MREQ signal should be used to do a refresh read to all dynamic memories. Output, active low.

Halt State (HALT) indicates the CPU has executed a HALT software instruction and is awaiting either a non-maskable or a maskable interrupt (with the mask enabled) before operation can resume. While halted, the CPU executes NOP's to maintain memory refresh activity. Output, active low.

Wait (WAIT) indicates to the Z-80A CPU that the addressed memory or I/O devices are not ready for a data transfer. The CPU continues to enter wait states for as long as this signal is active. Input, active low.

Interrupt Request (INT) signal is generated by I/O devices. A request will be honored at the end of the current instruction if the internal software controlled interrupt enable flip-flop (FF) is enabled. Input, active low.

Non Maskable Interrupt (NMI) request line has a higher priority than INT and is always recognized at the end of the current instruction, independent of the status of the interrupt enable flip-flop. NMI automatically forces the Z-80A CPU to restart to location 0066_H. Input, active low.

Reset initializes the CPU as follows: reset interrupt enable flip-flop, clear PC and registers I and R and set interrupt to 808A mode. During reset time, the address and data bus go to a high impedance state and all control output signals go to the inactive state. Input, active low.

Bus Request (BUSRQ) signal has a higher priority than NMI and is always recognized at the end of the current machine cycle. It is used to request the CPU address bus, data bus and tri-state output control signals to go to a high impedance state so that other devices can control these buses. Input, active low.

Bus Acknowledge (BUSAK) is used to indicate to the requesting device that the CPU address bus, data bus and tri-state control bus signals have been set to their high impedance state and the external device can now control these signals. Output, active low.

Video Display Processor

The VDP generates all video, control and synchronization signals and also controls the storage, retrieval and refresh of display data in a dynamic memory, VRAM.

For ColecoVision applications the VDP operates in a Graphics I mode. The Graphics I mode provides a 256 x 192 pixel display for generating pattern graphics in 15 colors plus transparent. A pixel is defined as the smallest point on the TV screen that can be independently controlled.

The video display consists of 35 planes; external VDP, backdrop, pattern plane, and 32 sprite planes. The planes are vertically stacked with the external VDP being the bottom or innermost plane. The backdrop plane is the next plane followed by the pattern plane that contains graphic patterns. The 32 top planes are sprite planes.

The VDP basically has three interfaces: CPU, RF modulator assembly, and a dynamic RAM (VRAM), the contents of which define the TV image. The VDP has eight write-only registers and a read-only status register.

The CPU interface consists of an eight bit bidirectional data bus, control lines and an interrupt.

Data can be transmitted to the CPU or from the CPU over the data bus, depending on the state of the CSW and CSR control lines. When CSW is low, data is transmitted from the CPU to the video display processor. When CSR is in a low state, data is transmitted from the video display processor to the CPU. CSR and CSW should not be simultaneously low.

Another control line, address line AØ, determines where the VDP will retrieve the data or where it will send the data. If AØ is high, the data will be stored into, or retrieved from an internal register. Which register is used is determined by the data. If AØ is in a low state the data will be stored into or retrieved from the VRAM.

The Video Display Processor has several internal registers, a general purpose eight bit data register, a 16 bit address register, and 8 eight bit dedicated purpose registers. The general purpose register is used to input

or output data on the CPU data bus. The address register inputs the address of the VRAM. The other eight registers store data for colors, images and image location.

The VDP accesses 16K bytes of dynamic ram called VRAM. The VRAM stores data to be used for image processing.

Three other functions are associated with the VDP; NMI, Reset and the clock. NMI provides a pulse to the CPU approximately every 1/60 second. Reset initializes the internal registers and the synchronization pulses to a known state. The clock input is a 10.7 MHz clock derived from the 3.58 MHz clock by using a third harmonic wave shaping circuit.

The Video Display Processor interfaces with eight 16K x 1 dynamic RAMS. This is accomplished by using two eight bit unidirectional busses and three control lines. Addressing the RAM is a two-step process. First RAS is active while an address is on the data-in/address bus. This is latched into the RAM and is used to select the Row address. The next step is to select the column. This is accomplished by strobing CAS low while an address is on the bus. The other control line R/W determines if data will be written into the VRAM or read onto the VRAM output bus. If R/W is low the data will be stored into RAM, if high the data will read from RAM to the output bus.

Memory

System ROM is arranged 8K x 8 bits. The CS in the low state reads data onto a data bus which is determined by a selected address. CS in the high state forces Q1-8 into a high impedance state (example: not connected to a bus.). It interfaces to the CPU using the U5 decoder.

Cartridge ROM has a memory capability of up to 32K x 8 bits that is selected in banks of 8K x 8 bits. Each bank is selected by CS1 — CS4 using the U5 decoder. CS 1 — CS4 is the same as chip select in system ROM.

RAM (Random Access Memory) has a memory capacity of 1K x 8 bits. RAM is comprised of two integrated circuits arranged 1K x 4 bits.
Write Enable Low writes DQ1-4 into the memory location selected by the address bus. Write Enable High reads DQ1-4 onto the data bus. DQ1-4 depends on data contained in the location selected by the address bus. Chip Select($\overline{S}$) High deselects the chip, DQ1-4 become a high impedance state, interfacing to the CPU using the U5 decoder and WR from the Z-80A.

RF Modulator

The RF Modulator interfaces video, color, difference, luminance and audio signals to the antenna terminal of the television receiver. It consists of a video modulator integrated circuit and associated discrete circuitry.

The discrete circuitry includes a sound tank circuit, a carrier frequency tank circuit and output impedance matching. An analog switch is used to switch in ColecoVision video or expansion module video. The analog switch is located on the main logic board, rather than on the RF board.

Hand Control Interface

The hand control interface consists of a spinner interface and a joystick/keypad interface.

The joystick/keypad interface uses two ground strobe outputs for each control port and five inputs for each control port. The ground strobe outputs are generated from the CPU address bus using a decoder and a flip-flop. The flip-flop ensures that one strobe is enabled at a time. One strobe is used for the joystick and to fire left. The other strobe is used for the keypad and to fire right. The inputs are buffered by two octal buffers, one for each port. At this point, a low input moves the character on the selected game. The buffers are gated onto the data bus by signals decoded from the address bus.

The spinner interface uses two inputs for each port. Required inputs are two square waves 180° out of phase. Phase relationship determines direction. Pulse time determines speed. One input is used to interrupt the microprocessor. This interrupt enables the microprocessor to halt its action, examine the square waves for direction and speed and then return to its original operation.

Power Supply

The entire power supply is contained in the plug-in wall unit. The supply contains a step-down transformer, rectifiers, filters and regulators. It outputs +5VDC, +12UDC and −5VDC.

The unit is ultrasonically welded, therefore it is not serviceable. If the power supply is defective or not working properly, the entire unit should be replaced.