The custom Video Interface Circuit (VIC) is an single N-Channel MOS LSI Integrated Circuit, which provides both analog and digital player inputs, Foreground, Moving Object, Projectiles, Border, and Audio Signals. The Microprocessor used in the system is the 6507. The ROMS used are the 2316 (16K) or 2332 (32K). The peripheral interfacing chip (PIC) is a 6532.

The game is Microprocessor controlled and each game definition is stored as a program in the ROM. The ROM contains the game rules, the score font, the object font, the background font or algorithm, and the sound algorithms. Each ROM can contain more than one game or variations of a game depending on game complexity.

The VIC develops Composite Video with Color Burst according to the NTSC video standard and uses a 3.579545 MHZ oscillator frequency supply by ColecoVision console. The display is non-interlaced. A block diagram of the system is shown in Figure 8A. The Microprocessor reads the stored program in the ROM and controls VIC to generate the video output. The VIC generates the Horizontal Sync, Horizontal Blanking, Color Burst, and Video Signals which contain the Color and Luminence signals. The Microprocessor keeps track of the number of horizontal lines scanned and controls the VIC to generate the Vertical Blanking and Sync. The VIC generates the sounds under control of the Microprocessor, which can control the frequency, shape, and amplitude.

The Microprocessor uses the PIC and VIC as the I/O interface for the player controllers (digital), player potentiometers (analog), and the front panel controls (digital). The system scratchpad RAM and Stack are in a 128 byte RAM in the PIC which also contains a programmable 8 bit timer.

The 128 byte RAM in the PIC is shared between the MPU stack and the system scratchpad RAM. The RAM is address transparent between $0080 thru $00FF and $0180 thru $01FF. This means that the same RAM appears in both of these address ranges simultaneously and care must be exercised not to let the stack alter the scratchpad RAM being used by the program.

8.2 SYSTEM MEMORY MAP

The following Memory Map outlines the System Memory for the Microcomputer System:

$F800-$FFFF	PROGRAM ROM HIGH (16K = 2K X 8)
$F000-$F7FF	PROGRAM ROM LOW (32K = 4K X 8)
$0280-$02FF	I/O INTERFACE & TIMER (PIC)
$0180-$01FF	STACK RAM (PAGE 1) (PIC)
$0080-$00FF	RAM (PAGE 0) (PIC)
$0000-$002C	VIC

The VIC is a Bus oriented device. The Microprocessor address and data busses enter the VIC and access the major functional areas. With the Address Bus the Microprocessor selects the area it desires to communicate with. The information is presented or received from the selected area on the Data Bus.

An external oscillator provides the 3.58 MHZ clock frequency for the VIC. The VIC then divides it by 3 to generate the clock for the Microprocessor.

The VIC internally generates the Horizontal Sync, Blanking, and Color Burst and genenates 4 displayable colors per line (Object A/Projectile A, Object B/Projectile B, Border/Foreground, and Background). Each color is independently programmable, and each one has a priority over the other. Some of the priorities can be altered by the Microprocessor. There are 128 Programmable colors for each of the above.

There are two fully programmable Objects (Object A and Object B). Each of these Objects is 8 bits wide and is fully programmable which means that there are 255 visible combinations of display for each Object. There are two Object Font Registers for each Object. Each Object Font Register contains one Byte (8 bits) of data. The direction in which the data is scanned can be reversed. The horizontal size of the bits in the Object display can be programmed to be 1, 2, or 4 units wide. Each of the Objects can be programmed to be repeated one or two times after the original and at different intervals from the original Object.

There are two dedicated objects (Projectile A and Projectile B) that are related to the main Objects (Object A and Object B). These

Projectiles can only be 1, 2, 4, or 8 units wide. Projectile A can be programmed to track the horizontal movement of Object A. Projectile B can be programmed to track the horizontal movement of Object B. The Projectiles can be repeated horizontally in conjunction with the associated Object. Projectile A is repeated exactly as Object A and Projectile B is repeated exactly as Object B.

There is also a dedicated object (Border) that can be moved or used as a ball, Border, or center line. The Border can only be 1, 2, 4, or 8 units wide. The Border cannot be repeated.

The Foreground is a 20 bit memory that can be displayed in one of four methods horizontally. Each bit is 4 units wide and the active foreground area is 160 units wide. The foreground memory acts as a register. The register is 2-1/2 bytes of RAM (20 bits). The foreground register is displayed two times each line (40 bits/line).

An object can be made to appear over or under the Foreground and Border and can appear over or under another object based on a priority system. Object A, Object B, Projectile A, and Projectile B can be programmed as higher or lower priority than the Foreground and Border. Object A and Projectile A are always a higher priority than Object B and Projectile B.

The horizontal movement of each Object (A and B), Projectile (A and B), and the Border is controlled by the Microprocessor. Each of these 5 can be moved left or right relative to the Horizontal Reference Counter. Movement can be from -7 to +8 horizontal units per horizontal line sweep.

The VIC has a coincidence detection circuit that indicates when any two Objects, Projectiles, Foreground, Border, or any combination of

the above are coincidental with each other. A set of 15 comparators compares each object against the other and stores the result in a set of registers which can be read and reset by the Microprocessor.

The VIC has 4 analog inputs with Schmitt triggers for accurate repeat detection of the player potentiometer setting. The analog inputs use a resistor-capacitor circuit for the time constant; the resistor is a potentiometer that is controlled by the player. Each input has a programmable discharge transistor that can be turned on to discharge the capacitor in the RC timing circuit.

There are also 2 Trigger inputs which can be used as latching Input Ports. Whenever one of these inputs goes to a "0" level, this transition is stored in a latch that can be reset under software control. The latching mode is programmable and when turned off the data at the Trigger inputs is passed directly to the MPU when read.

The VIC contains two Sound generators each of the Sound generators are connected to one of the two Sound Output pins.

The Sound Generator consists of a Programmable Divider that divides the horizontal sweep frequency, a Sound Generator, and a programmable Output Driver. The Divider can be programmed to divide the 15.7 KHZ horizontal sweep frequency by 1 to 32. The Sound Circuit is programmable for 10 different sounds and tones. This circuit can produce a series of sounds from a simple tone to a complex random noise. The Output Driver can be programmed for 15 different output levels.

8.31 VIC GENERAL FEATURES

* 2 General Purpose Objects
* 3 Dedicated Objects
* Object Duplication (2 Programmable Repeat Objects)
* Object Size and Movement Under Microprocessor Control
* Programmable Object Priority
* 280 nsec Object Resolution
* Programmable Foreground
* Programmable Foreground Repeat or Mirroring
* 128 Programmable Colors
* Programmable Vertical Sync and Vetical Blanking Timing
* 2 Programmable Sound Generators
* 4 Analog Potentiometer Inputs
* 2 Digital Inputs (Edge Sensitive Programmable)
* 4 Displayable Colors per Horizontal Scan Line
* 4 Chip Select Lines for Address Decoding
* 40 Pin Dual-In-Line Package
* Page Zero Microprocessor Operation

8.32 The following is a summary of the input and output pins of the E4002 and their electrical characteristics for VCC/5.0V ±0.25V for TA/0-70°C.

Pin 1 Gnd.

Pin 2 Øo output push-pull output driver VOL/0.4V at 1.6mA VOH/-100.0uA at 2.4V signal is osc input divided by 3 and drives the Ø0 input of the 6507 (Pin 27).

Pin 3 RDY output drain output that pulls to GND VOL/0.4V at 1.6mA IOH/10.00uA at 5.25V. This pin drives RDY input (Pin 3) of 6507. Has a 4.7K pullup resistor (external) to VCC.

Pin 4 Sync output open drain output that pulls to GND VOL/0.4V at 1.6mA IOH/10.0uA at 5.25V. This pin is the horizontal and vertical sync output. Has a 3.3K pullup to VCC.

Pin 5, 6,7,8, and 9

LUM and blanking outputs same electrical parameters as pin 4. Pin 5 is LUM4, pin 6 is LUM2, pin 7 is LUM1, and pin 8 is BLNKG. Pin 9 color burst output same electrical parameters as pin 4 except a 1K pullup to VCC is used. This pin generates the color burst reference during horizontal blanking and the color burst during the active display lines.

Pin 10 Color adjust an input that is used to adjust the phase shift network for the color generator. This is a D.C. voltage. IIN/10.0uA max. VIN/o to 6V.

Pin 11 Oscillator input. 3,579,545 HZ input. Input levels 0/0.4V 1/4.0V 50 pct duty cycle ±10%. Trise, Tfall less than 30N sec.

Pin 12, 13, 14, 15, 16, and 17

DB0 thru DB5 inputs VINL/0.4V VINH/2.4V IIN/10.0uA. These pins are connected to the 6507 DB0 thru DB5 outputs.

Pin 18, 19,

DB6, DB7 input/output pins. Tristate Outputs. Tristate input/10uA outputs on VOL/0.4V at 1.6mA, VOH/2.4V at 100uA.

Pin 20 VCC 5.25V to 4.75V 5.0V nom. ICC max 120.0mA.

Pin 21, 22, 23, and 24

Chip select inputs IIN/10.0uA.

Pin 25 R/W input IIN/10.0uA connected to 6507 R/W output (Pin 26).

Pin 26 Ø2 input IIN/10.0uA connected to 6507 Ø2 ouput (Pin 28).

Pin 27 and 28

Sound output pins connected together in system and connected together to a 1K pullup resistor to VCC. Each pin has 4 open drain output transistors binary weighted at 2.5K, 5.0K, 10.0K, and 20.0K plus or minus 20 pct with 1.0V VDS. Matching within 6 pct. IOH/10.0UA.

Pin 29, 30, 31, 32, 33, and 34

Address inputs AB thru AB5 connected to 6507 address lines. IIN/10.0UA.

Pin 35, 36

TGR1 and TGR2 inputs IIN/10.0US These inputs have Schmitt trigger inputs with approx 100 MV hysterisis min. and a trip point of approx 2.5V.

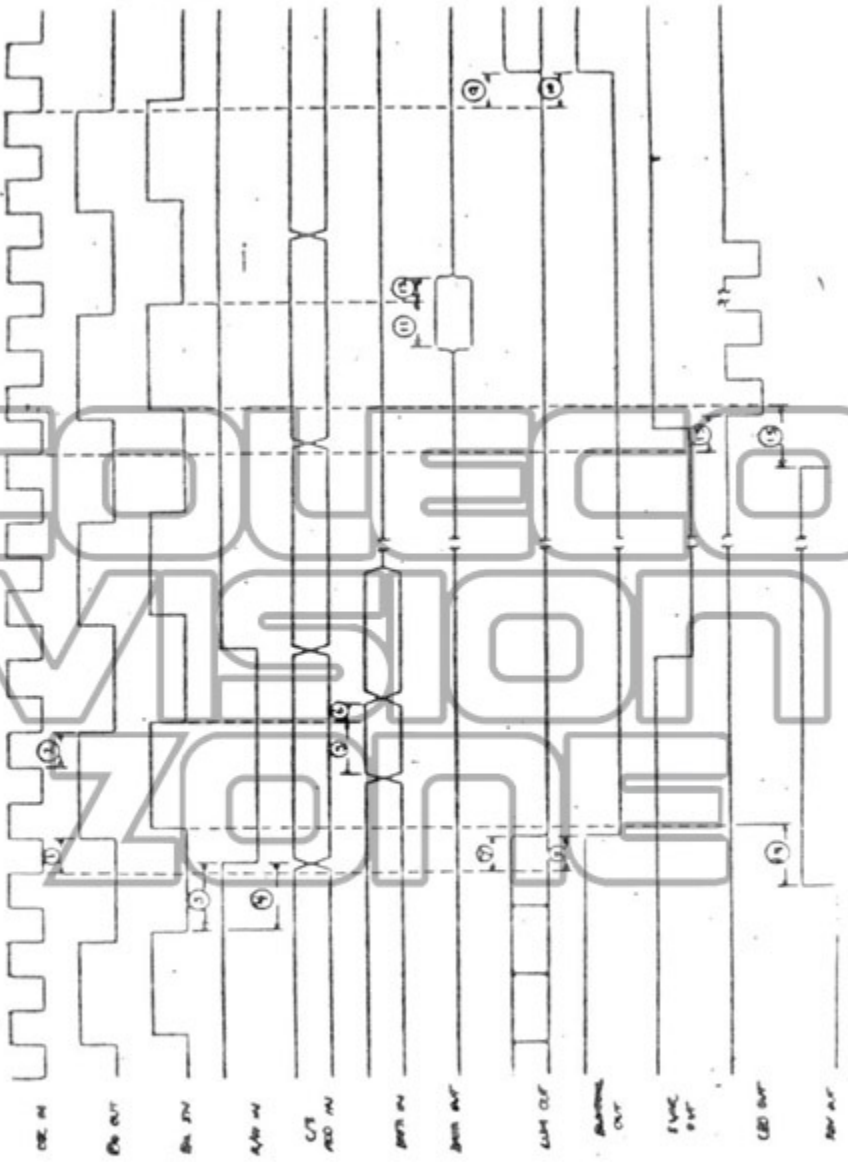
Pin 37, 38, 39, and 40

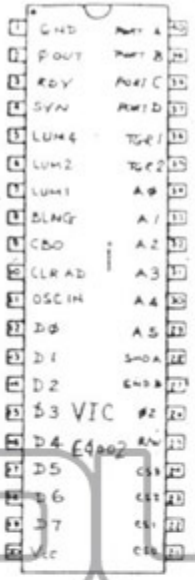
Potentiometer inputs same as pins 35 and 36 except for an open drain discharge transistor. IOL/250 US at 0.4V IOH/10.0 US.

8.33 E4002 TIMING SPECIFICATIONS

(1)	OSC IN to ϕ_0 OUT "1"	200 nsec
(2)	OSC IN to ϕ_0 OUT "0"	200 nsec
(3)	ϕ_2 IN to R/W	300 nsec
(4)	ϕ_2 IN to ADD & C/S IN	300 nsec
(5)	DATA IN to ϕ_2 IN DATA (DATA SET-UP)	200 nsec
(6)	ϕ_2 IN to DATA IN (DATA HOLD)	30 nsec
(7)	OSC IN to LUM OUT "0"	200 nsec
(8)	OSC IN to BLANKING OUT "0"	200 nsec
(9)	OSC IN to LUM OUT "1"	200 nsec
(10)	OSC IN to BLANKING OUT "1"	200 nsec
(11)	DATA OUT to ϕ_2 IN "0" (DATA SET-UP)	200 nsec
(12)	ϕ_2 IN to DATA OUT (DATA HOLD)	50 nsec
(13)	OSC IN to COLOR BURST OUT (REF)	200 nsec
(14)	RDY OUT "1" to ϕ_2 IN "1"	200 nsec
(15)	RDY OUT "0" to ϕ_2 IN "1"	200 nsec

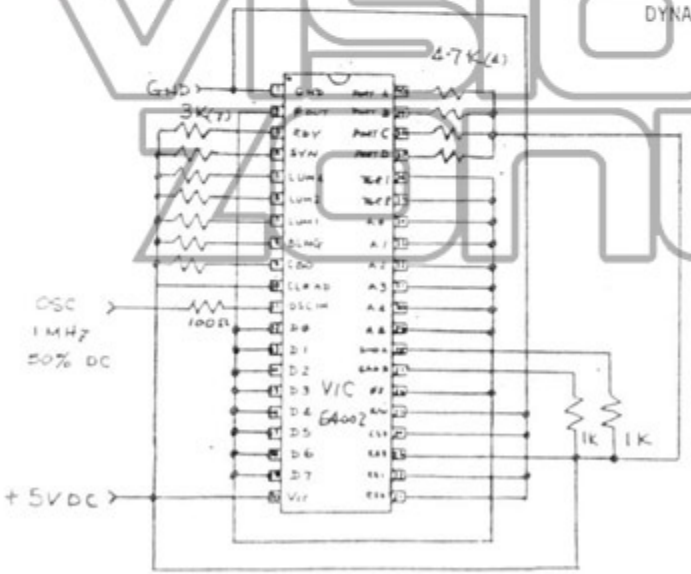
E4002





E4002 PIN OUT

DYNAMIC BURN-IN CIRCUIT



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