CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT
Input High Voltage Logic, $\Phi_{1,2}$ (in)	V_{IH}	V_{SS} + 2.4	—	V_{CC}	Vdc
			—		Vdc
Input High Voltage $\overline{RES}$, $\overline{NMI}$, RDY, $\overline{IRQ}$, Data, S.O.		V_{SS} + 2.0	—	—	Vdc
Input Low Voltage Logic, $\Phi_{1,2}$ (in)	V_{IL}	V_{SS} − 0.3	—	V_{SS} + 0.4	Vdc
		—	—		
$\overline{RES}$, $\overline{NMI}$, RDY, $\overline{IRQ}$, Data, S.O.		—	—	V_{SS} + 0.8	Vdc
Input Leakage Current (V_{in} = 0 to 5.25V, V_{CC} = 5.25V) Logic (Except RDY, S.O.)	I_{in}	—	—	2.5	μA
		—	—		
$\Phi_{1,2}$ (in)		—	—	100	μA
Three State (Off State) Input Current (V_{in} = 0.4 to 2.4V, V_{CC} = 5.25V) Data Lines	I_{TSI}	—	—	10	μA
Output High Voltage (I_{OH} = −100μAdc, V_{CC} = 4.75V) SYNC, Data, A0-A15, R/W	V_{OH}	V_{SS} + 2.4	—	—	Vdc
Out Low Voltage (I_{OL} = 1.6mAdc, V_{CC} = 4.75V) SYNC, Data, A0-A15, R/W	V_{OL}	—	—	V_{SS} + 0.4	Vdc

TABLE 7A - I/O Specification

READ/WRITE TIMING (LOAD = 1TTL)

Unit/ns

CHARACTERISTIC	SYMBOL	MIN	TYP	MAX
Read/Write Setup Time from 6507	T_{RWS}	—	100	300
Address Setup Time from 6507	T_{ADS}	—	100	300
Memory Read Access Time	T_{ADC}	—	—	575
Data Stability Time Period	T_{DSU}	100	—	—
Data Hold Time—Read	T_{HR}	10	—	—
Data Hold Time—Write	T_{HW}	30	60	—
Data Setup Time from 6507	T_{MDS}	—	150	300
R/D Setup Time	$T_{R/D}$	100	—	—
SYNC Setup Time from 6507	T_{SYNC}	—	—	300
Address Hold Time	T_{HA}	30	60	—
R/W Hold Time	T_{HRW}	30	60	—
RDY Setup Time	T_{RDY}	100	—	—

CLOCK TIMING — 6507

Unit/ns

CHARACTERISTIC	SYMBOL	MIN	TYP	MAX
Cycle Time	T_{CYC}	1000	—	—
$\Phi_{0(in)}$ Pulse Width (measured at 1.5V)	$PWH\Phi_0$	480	—	520
$\Phi_{0(in)}$ Rise, Fall Time	$T_{RF\Phi_0}$	—	—	10
Delay Time between Clocks (measured at 1.5V)	T_D	0	—	—
$\Phi_{1(OUT)}$ Pulse Width (measured at 1.5V)	$PWH\Phi_1$	$PWH\Phi_{0H} - 40$	—	$PWH\Phi_{0H} - 10$
$\Phi_{1(OUT)}$ Rise, Fall Time (measured at 0.2V, 6.4V in 1 TTL)	T_F, T_R	—	—	25

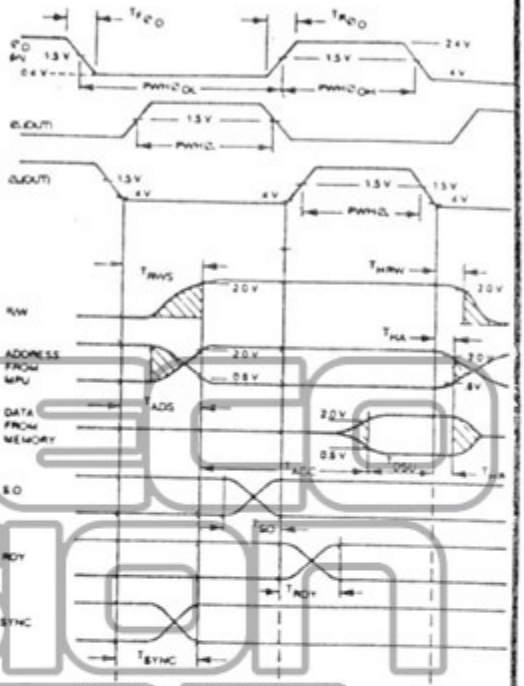


TABLE 7B - Timing Table

7.65 Hand Controller Connector J3 and J4

J3 Left Connector		J4 Right Connector	
Pin 1	PA4 I/O Table 7C	Pin 1	PA0 I/O Table 7C
Pin 2	PA5 I/O Table 7C	Pin 2	PA1 I/O Table 7C
Pin 3	PA6 I/O Table 7C	Pin 3	PA2 I/O Table 7C
Pin 4	PA7 I/O Table 7C	Pin 4	PA3 I/O Table 7C
Pin 5	Port A Input Item 8.32, Pin 10	Pin 5	Port C Input, Item Pin 35
Pin 6	Trg 1 Input Item 8.32, Pin 36	Pin 6	Trg 2 Input, Item Pin 35
Pin 7	+5V	Pin 7	+5V
Pin 8	-0.3V Negative bias	Pin 8	-0.3V negative bias
Pin 9	Port B Input, Item 8.32, Pin 39	Pin 9	Port D Input, Item 8.32, Pin 37

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT
Input High Voltage	V_{IH}	V_{SS} + 2.4	—	VCC	V
Input Low Voltage	V_{IL}	V_{SS} - .3	—	V_{SS} + .4	V
Input High Current, V_{IN} = 2.4v PA0-PA7, PB0-PB7	I_{IH}	- 100	- 300	—	µA
Input Low Current, V_{IN} = .4v PA0-PA7, PB0-PB7	I_{IL}	—	- 1.0	- 1.6	mA
Output High Voltage VCC = MIN. $I_{LOAD} \leq$ -100µA (PA0-PA7, PB0-PB7, D0-D7) $I_{LOAD} \leq$ -1mA (PB0-PB7)	V_{OH}	V_{SS} + 2.4 V_{SS} + 1.5	—	VCC	V
Output Low Voltage VCC = MIN. $I_{LOAD} \leq$ 1.6MA	V_{OL}	V_{SS}	—	V_{SS} + .4	V
Output High Current (Sourcing) VOH ≥ 2.4v (PA0-PA7, PB0-PB7, D0-D7) ≥ 1.5v Available for other than TTL (Darlingtons) (PB0-PB7)	I_{OH}	- 100 - 3.0	- 1000 - 6.0	—	µA mA
Output Low Current (Sinking) VOL ≤ .4v (PA0-PA7) (PB0-PB7)	I_{OL}	1.6	—	—	mA

Table 7C, I/O Specification

7.7 System Performance Test Specification

Test cartridge number 92064 is used for following system performance test. Press game select switch advances each test.

7.71 Test #1: Color Adjust Screen

Power up, test cartridge inserted; set color, adjust potentiometer so that left side of screen is the same color as right side of screen. Initially right side of screen should be green. Deviation of left side green, relative to right side green may be determined from provided certified standards, which determine the extent left side of screen may safety deviate from right side of screen and still allow true color presentation.

The result of the data line and address line test is displayed in the region above and below the color bars. The left side indicates the result of the data line test. The right side indicates the result of the address line and RAM test, when both of the regions are green then the tests were both passed, when either one is red, this indicates a failure of that test. See figure 7.71A.

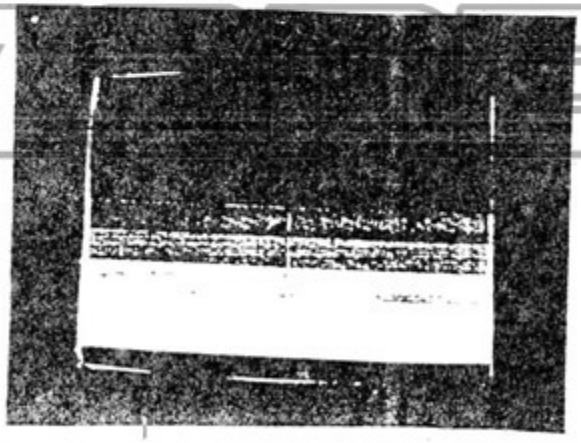


figure 7.71A
Color Adjust Screen

7.72 Test #2: Color Display Test

See Figure 7.72A.

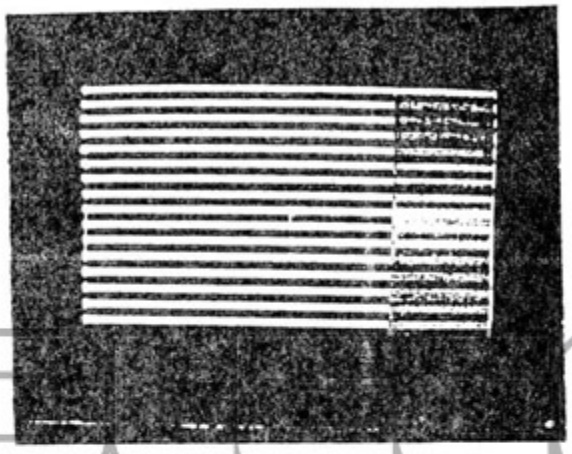


Figure 7.72A Color Display Screen

7.73 Test #3: Coincidence Test

Displays a series lines down the left side and 2 sets of 5 blue squares on the left and center of the screen. If the test is passed the top and bottom of the screen will be green, if the test fails, a large blue pair of stripes will appear where the failure took place and the top and bottom of the screen will be red. See figure 7.73A.

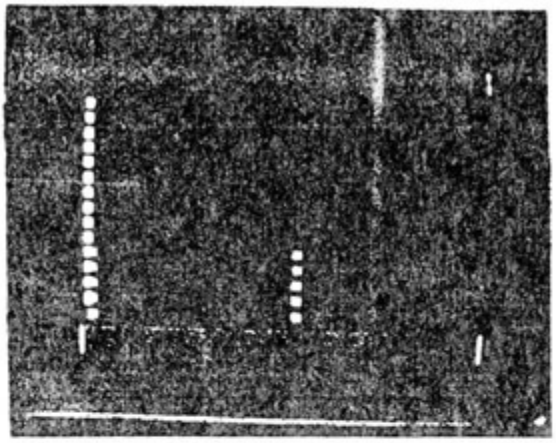


Figure 7.73A
Coincidence Test Screen

7.74A Test #4: Foreground Display Test

See figure 7.74A.

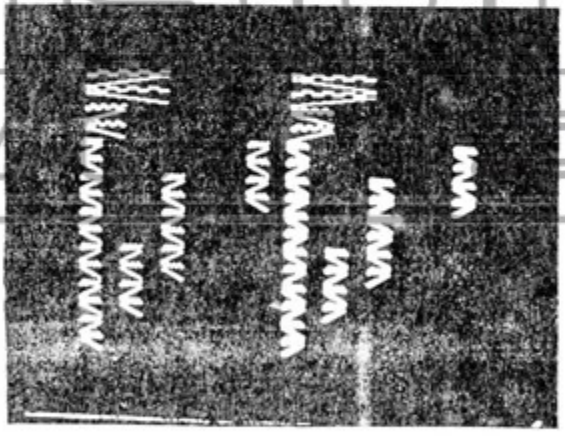


Figure 7.74A
Foreground Display Test

7.75 Test #5: Object Display Test

See Figure 7.75A

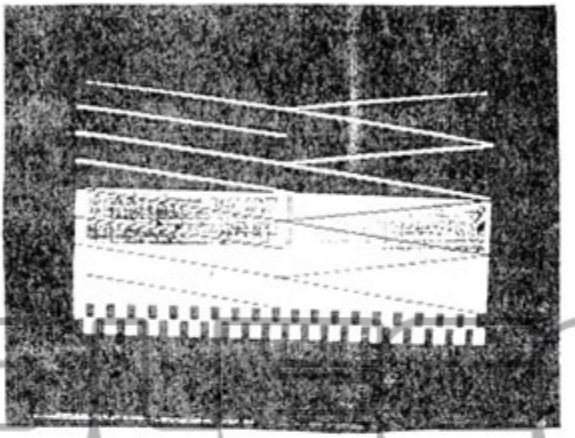


Figure 7.75A

Object Display Screen

7.76 Test #6: Projectile and Border Test

Also test Object Priority and Projectile Tracking.

See Figure 7.76A.

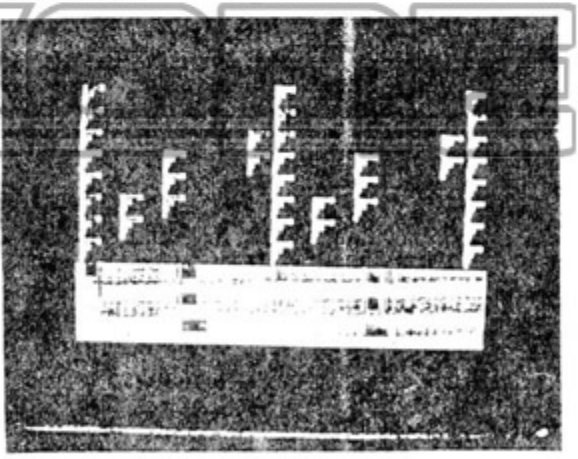


Figure 7.76A

Projectile and Border Test Screen

7.77 Test #7: Sound Test

An feedback circuit Figure 7.77A shall be installed to test sound output. A fail-screen 7.77B and pass-screen 7.77C shall be displayed.

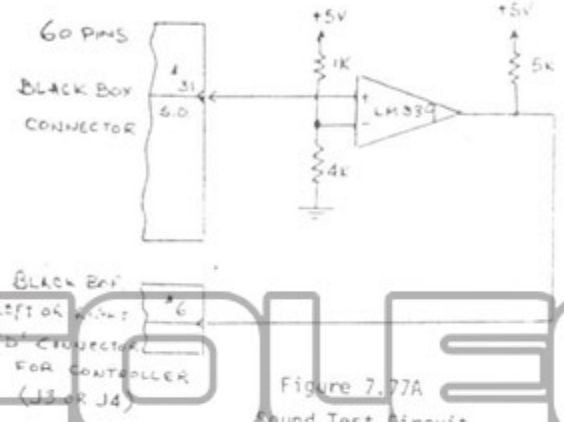
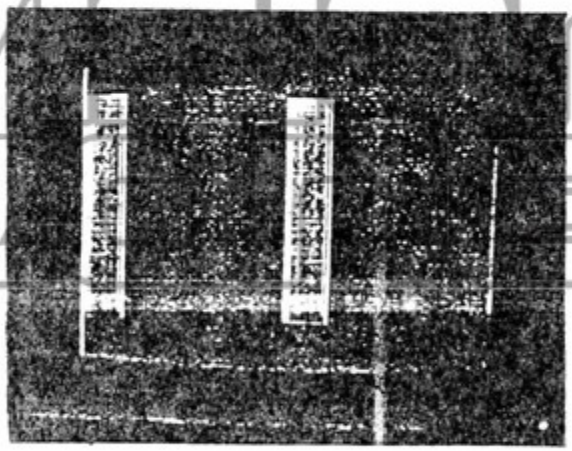
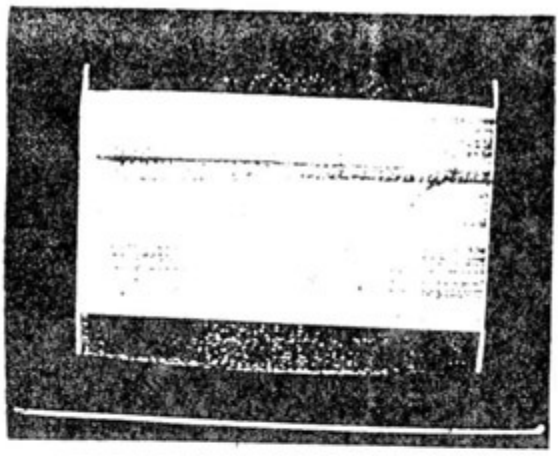


Figure 7.77A
Sound Test Circuit



7.77B Sound Test Fail Screen



7.77C Sound Test Pass Screen

7.78 Test #8: I/O and Switches Test

A test circuit, constructed per Figure 7.78A, shall be connected to the two 'D' connectors for controllers. After the connection of the test circuit, Figure 7.78B shall be displayed. After activation of Black-White/Color, two difficult slide switches and game reset push button switch, Figure 7.78C is displayed.

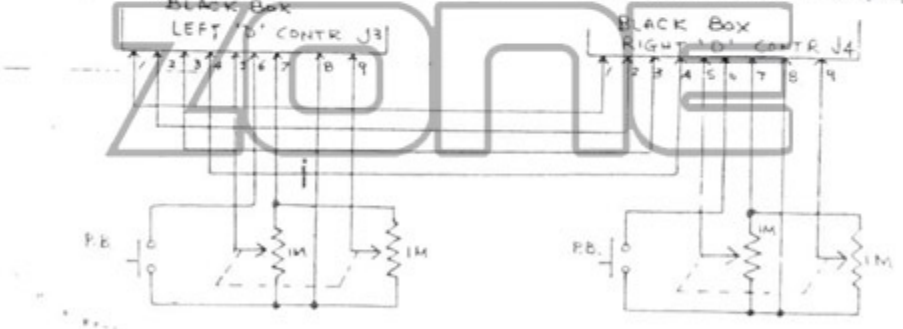


Figure 7.78A
Connector Test Circuit

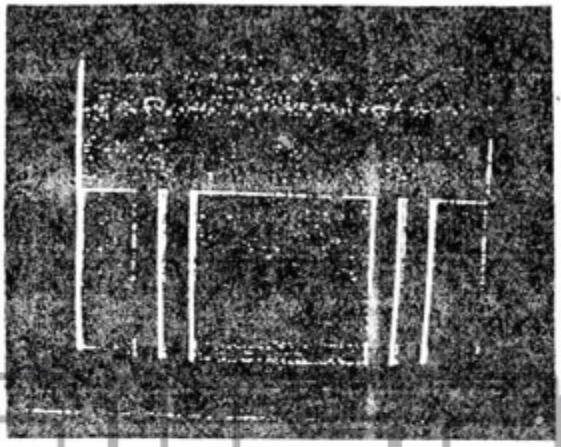


Figure 7.78B
I/O Test Screen

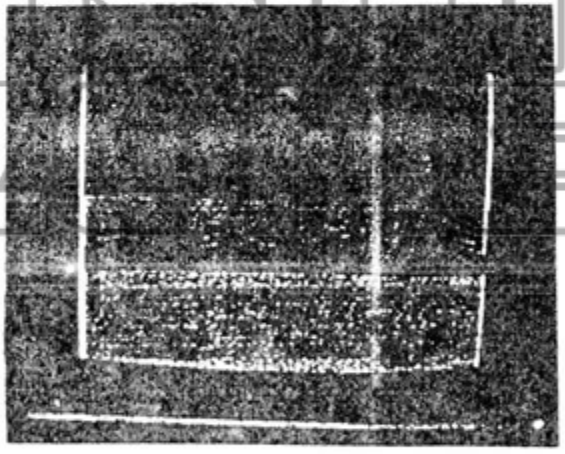


Figure 7.78C
I/O Test Screen Pass

Circuit 7.78A is also used in this test. Test screen 7.79A is displayed initially. Activation of two trigger buttons of circuit 7.78A should eliminate two vertical lines at each side. Turning the two potentiometers should moving the middle lines up or down.

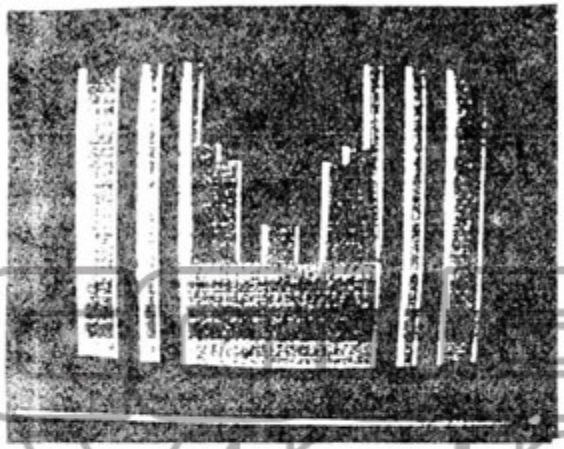


Figure 7.79
Pot and Trigger Test Screen

7.710 Test #10: Delayed Register Test

See figure 7.710A for display. A green top and bottom screen is displayed after passing all previous test. Red screen results when one or more previous tests fail.

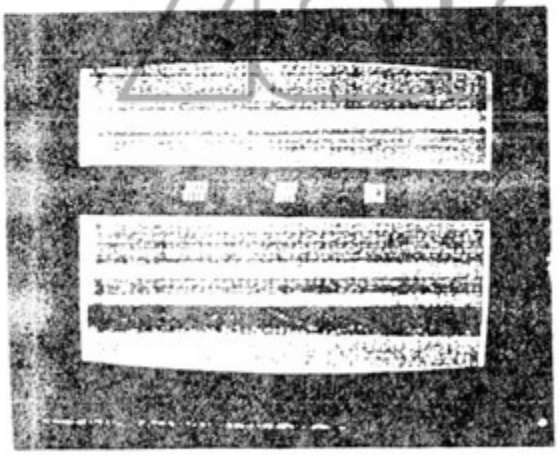


Figure 7.710A
Delayed Register Test

8. PRODUCT DESCRIPTION

The sole purpose of this expansion module is to provide interface between 'A' cartridges and ColecoVision console. Spring - return lid protects 24 pin female edge connector which is used for acception of 'A' cartridges. 60 pin female edge connector located at back side provides electrical and mechanical link between expansion module and ColecoVision console.

The Black box has two 9-pin male "D" connectors located at the front for connection of either ColecoVision or 'A' controllers.

Color-B/W slide switch is used to switch system to be compatible with black and white TV set. Two slide switches labeled LEFT DIFF. and RIGHT DIFF. are used to select difficulties levels for left and right controllers.

Momentary "SELECT" switch allows player to select games and "RESET" switch to reset/start games. In addition the ColecoVision console "RESET" switch specifically provides hardware reset to the Black Box.

8.1 Technical System Description

A PCB, fully shielded to FCC part 15 requirement, consist of three major systems, namely 6507 CPU System, 6532 - RAM - I/O - TIMER (RIOT) and custom video display generator E4002. System clock 3.58 MHZ is supplied by ColecoVision console via the edge connector.

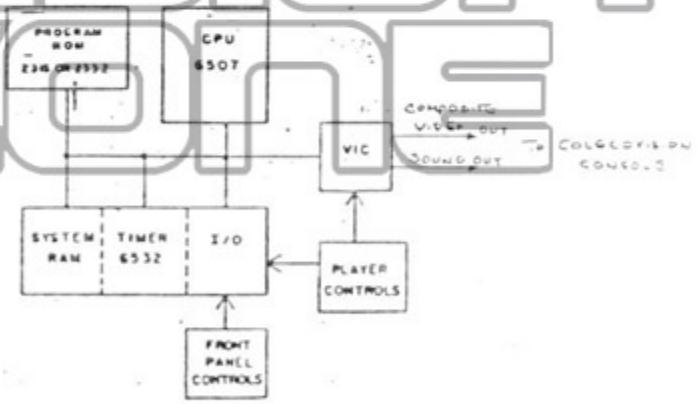


FIGURE 6

EXPANSION MODULE #1